High Input-impedance Amplifier Circuits

Using bipolar transistors, integrated circuits and f.e.ts in a.c. amplifiers presenting low loading on the signal source.

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In the ordinary course, engineers do not find many requirements for low-frequency, high input-impedance amplifiers. This is fortunate, because the "ordinary" bipolar transistor, with which they have done most of their circuitry for a decade now, is basically a low-impedance device. The "old-fashioned" thermionic valve had one big advantage; with comparatively simple circuit arrangements you could easily achieve input impedances of over 100MΩ. With bipolar transistors, quite specialized circuits had to be devised to get above even 100kΩ. But things are changing again; we are moving into an age where the f.e.t. and the monolithic integrated circuit are displacing bipolar transistors—just as transistors did valves.

High input impedance with bipolar transistors

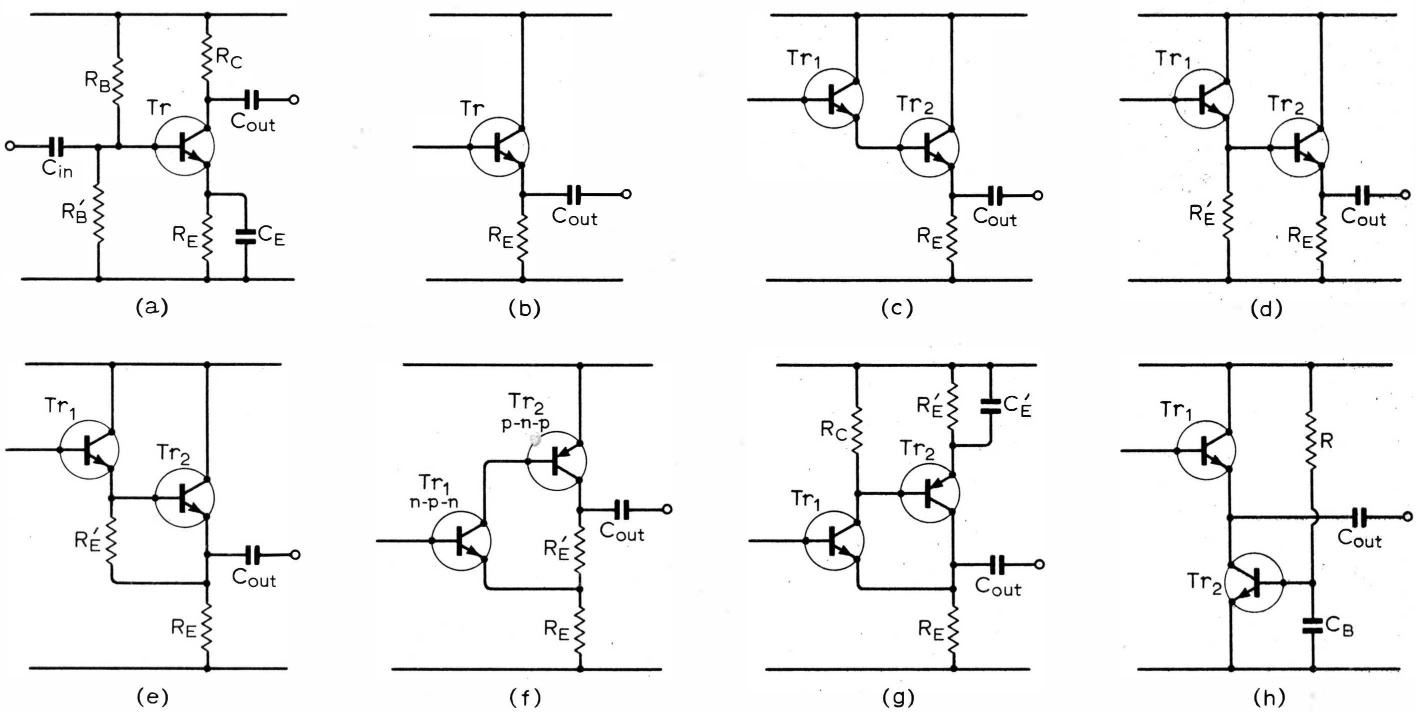
Consider the conventional common-emitter amplifier stage shown in Fig. 1(a). At frequencies where the input and output coupling and the emitter decoupling capacitors present negligible impedance, three factors control the low-frequency impedance seen looking into the amplifier input terminal. These are the shunt impedances presented by the emitter circuit, by the base-bias resistors and by the collector circuit, all in parallel across the input (both positive and negative supply rails being a.c. grounded).

Emitter circuit shunt impedance: So far as it is governed by the emitter circuit, the low frequency input impedance of the transistor itself is given approximately by $R_{in}=r_{bb'}+25h_{fe}/I_E$, where $r_{bb'}$ is the device "base spreading resistance" (for transistors used in low-level circuits usually 30 to 300Ω), h_{fe} is the common-emitter current gain (nowadays usually 50 to 250), and I_E is the emitter current in mA. For a typical low-level stage with I_E set about 1mA, we find R_{in} typically 1 to 2kΩ. The formula for R_{in} shows that you can increase the device input impedance by reducing the emitter current, provided current gain does not fall at the same time. With germanium transistors, h_{fe} tended to fall almost linearly with current below 1mA, so that little use could be made of reducing the emitter current to put up input impedance. Modern silicon transistors generally hold up their current gain to much lower current levels than germanium. With devices of the common BC107, 8, 9 family, for example, a current gain of 100 at 100μA makes possible a transistor a.f. input resistance of 25-50kΩ.

High input impedance with input transformer or series resistor: Before we go on to examine other high-impedance circuit arrangements, we should not forget that you can use a transformer with a high step-down turns ratio. Such a transformer has the advantage of isolation, but, to get high impedance at low frequencies, its size and cost can become prohibitive. The upper frequency limit may

tances. Careful screening is called for, and it is sometimes difficult to provide simultaneously minimum noise and high impedance.

Fig. 1. Arrangements for reducing shunting of emitter circuits on transistor input impedance. (a) Basic common-emitter amplifier operated at low bias current. (b) Common-collector (emitter-follower) single transistor. (c) Compound two-transistor Darlington-pair common-collector. (d) Modified Darlington-pair common-collector. (e) Bootstrapped Darlington-pair. (f) and (g) Complementary n-p-n/p-n-p compound emitter-follower circuits. (h) Transistor-loaded emitter-follower.



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*Newmarket Transistors Ltd.

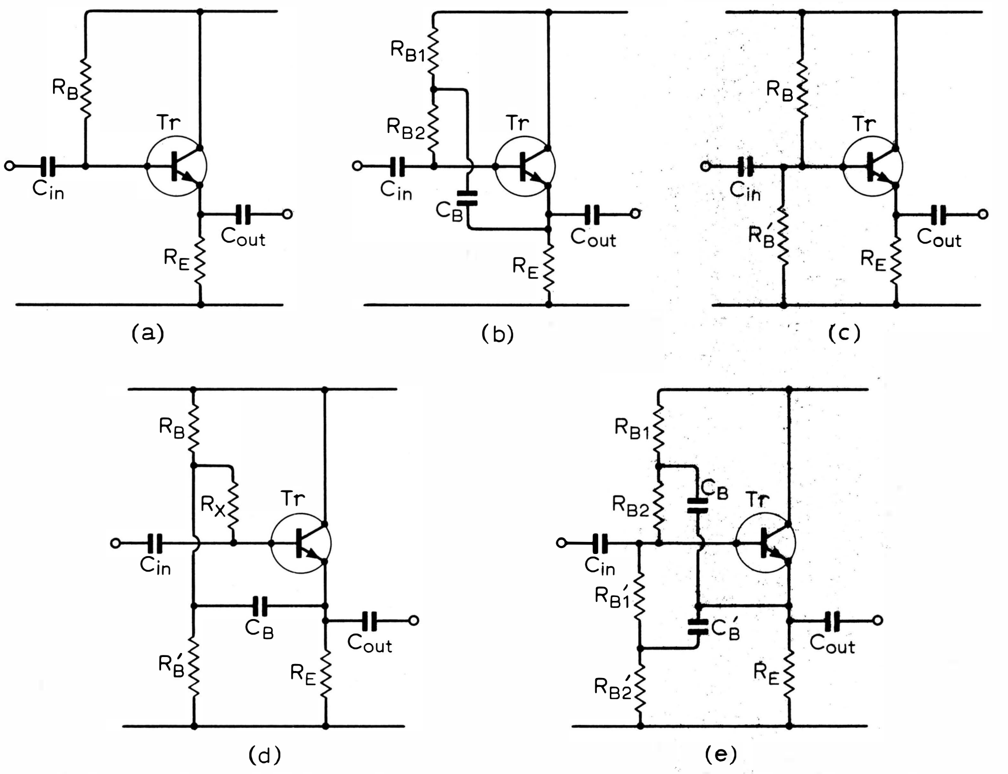


Fig. 2. Reducing the shunting of base bias resistors on input impedance. (a) Basic single-resistor transistor bias circuit. (b) Bootstrapping single bias resistor by capacitance feedback to its centre. (c) Basic two-resistor base bias circuit. (d) Single-capacitor method of bootstrapping two-resistor bias network. (e) Two-capacitor method of bootstrapping two-resistor bias network.

One other simple approach is to accept the intrinsic low input resistance of the transistor and achieve the required high input resistance by using a series resistor to the input. The main objection to this is the high noise level likely to arise from the large value series resistor.

Reducing shunting effect of emitter circuits on input impedance: Going back to the common-emitter stage of Fig. 1(a), if we remove the emitter bias resistor decoupling capacitance, C_E, the transistor input impedance becomes $R_{in}=r_{bb}+h_{fe}\,(25/I_E+R_E)$. This shows that we can increase the input impedance by using an undecoupled emitter resistor. It would seem that you could increase R_{in} indefinitely by increasing R_E, but, when R_E rises above about one-tenth of the collector load resistance, R_C, the voltage gain of the common-emitter stage approaches R_C/R_E. The gain thus falls to unity when $R_E=R_C$. This is why designers looking for high transistor input impedance tend to use the alternative near-unity-gain common-collector arrangement of Fig. 1 (b). By using silicon transistors with high gain at low current, it is possible to increase R_E to a value giving input impedances of the order of several thousand ohms with this simple arrangement.

Unless you go to a very high rail voltage, even when you resort to low bias currents, you are limited in how high you can raise the value of R_E. You can get round this with the Darlington compound-emitter-follower arrangement of Fig. 1(c). Here, then; $R_{in}=h_{fe1}h_{fe2}R_E$ approx., and you can see that a.c.-wise by adding the extra transistor you have effectively multiplied R_E by h_{fe2} without raising its d.c. value, and thus without having to go to a higher rail voltage. The emitter current of Tr_1, being the base current of Tr_2, is usually low: typically of the order of 1-5μA only. Tr_1 should be a transistor with high gain at low current, such as the 2N930 with h_{fe} greater than 100 at 10μA. Some designers raise the standing current in Tr_1 with a separate emitter bias resistor, $R_{E'}$, in Fig. 1(d). This shunts the input impedance of Tr_2, but its shunt effect on the overall input impedance may be more than offset by the increase in h_{fe1} due to the higher Tr_1 bias current. Usually $R_{E'}$ is made 5 to 20 times R_E.

To reduce the loading of R_E on the input, you can use the bootstrap feedback arrangement of Fig. 1(e), where the bottom of $R_{E'}$ is connected to the top of R_E. By the emitter-follower action of Tr_2, the lower end of $R_{E'}$ moves with its top, and its resistance value is effectively multiplied by the current gain of Tr_2 (provided, as is usually the case, R_E is small compared with $R_{E'}$). With silicon transistors, the V_{BE} (d.c.) of Tr_2 is approximately 0.6V, so that $R_{E'}$ is fixed by the selected bias current, I_{E1}, of Tr_1 as $R_{E'}=0.6/I_{E'}$ (ignoring the negligible base current into Tr_2).

Combinations of n-p-n and p-n-p transistors permit other arrangements for bootstrapping up the effective value of the emitter resistor in an emitter follower. For example, in both Fig. 1(f) and 1(g), it can be shown that R_{in} has a high value give approximately by $R_{in}=h_{fe1}\,h_{fe2}\,R_E$.

Another elegant circuit for providing a high-resistance emitter load in an emitter-follower without high rail voltages is shown in Fig. 1(h). Here the output resistance of Tr_2 (of the order of megohms) functions as an emitter load to Tr_1 and makes possible an overall input resistance over 10MΩ.

Reducing shunting effect of base bias resistors on input impedance: So far, we have ignored the effect on input impedance of any base bias resistor networks shunted across the transistor input. Fig. 2(a), showing an elementary single-resistor bias circuit, illustrates the problem. You will see that R_B is directly across the input (both supply rails being a.c. earthed). Obviously the total R_{in} cannot exceed R_B.

The conventional technique to raise the effective a.c. resistance of R_B without raising its d.c. value is to bootstrap it as shown in Fig. 2(b). R_B is replaced by two resistances R_{B1} and R_{B2} of the same total resistance. Provided R_{B1} and R_{B2} are large compared with R_E, the transistor emitter-follower action makes the top end of R_{B2} move up and down with its bottom end. Thus its a.c. impedance is raised effectively by the current gain of the transistor.

The more thermally-stable conventional two-resistor bias network of Fig. 2(c) can also be bootstrapped for high impedance. Fig. 2(d) shows an arrangement using a single bootstrap capacitor, C_B, in which the resistance R_X in series with the base can be low value for thermal stability, but have high effective impedance so as not to shunt the input a.c. signal. Fig. 2(e) shows a two-capacitor arrangement where both top and bottom bias resistors are capacitor-bootstrapped by splitting each as explained for Fig. 2(b) above.

In general, the bootstrap capacitance values must be large enough to present negligible impedance at the lowest frequency, f_o, to be handled. A useful guide is to make C_B greater than $10/(f_oR_B)$, where R_B is the bias resistor being bootstrapped.

Reducing shunting effect of transistor collector output resistance: From the conventional low-frequency T-equivalent circuit of the transistor in the common-collector configuration with emitter resistor, R_E, shown in Fig. 3(a), you can see that the internal collector resistance, r_c, shunts the signal path. At low current levels with modern transistors, r_c usually lies between 1 and 5MΩ, so that it is difficult to reach higher input impedances than r_c unless it too is bootstrapped. Fig. 3(b) shows the basic arrangement for this, where a resistance, R_C, is inserted between the collector and h.t. (to isolate r_c from earth a.c.-wise) and a capacitor, C_F, to the collector (and thus the outer end of r_c) feeds back in phase signals from the top end of the emitter resistance. This raises the effective a.c. impedance of r_c and reduces its shunting effect on the input signal. If possible, the collector bias resistance, R_C, value should be at least ten times R_E, but, if only a limited d.c. supply voltage is available, this may not be possible, unless we are using a multiple emitter-follower, as explained previously in Figs. 1(c)-(e), where R_E is relatively small.

Fig. 3(c) illustrates a circuit using a separate transistor, Tr_2, to bootstrap the Tr_1 collector output resistance without excessive loading of its emitter output. The a.c. voltage at the top of R_E is transferred via C_F and the base-emitter of Tr_2 to the collector of Tr_1.

It is also possible to bootstrap the base bias resistor and the collector output resistance at the same time with a single capacitor as in the simple circuit arrangement of Fig. 3(d).

One aspect of bootstrapping with capacitors is that high input impedance circuits tend to be operated at low transistor bias currents, and the leakage currents in ordinary aluminium electrolytic capacitors can upset bias conditions drastically. For this reason, you will often find low-leakage tantalum capacitors specified, where the total capacitance required is beyond the range of solid dielectric types.

Practical high-impedance transistor amplifiers: Fig. 4(a) shows a simple single-transistor, emitter-follower, high input impedance amplifier operating at a low collector current of about 100μA, and with bootstrapping of base-bias resistors and collector output resistance. These techniques produce an input impedance down to below 50Hz not less than 0.5MΩ.

For input impedances greater than about 1MΩ, usually two stages are necessary with bipolar transistors. Fig. 4(b) is a typical circuit with an input resistance of 1.5MΩ and an output resistance of only 30Ω. It employs an n-p-n/p-n-p direct-coupled pair with bootstrapping of base bias resistors and emitter resistor.

Two stages can give an input impedance of the order of 10MΩ, as, for example, the cascaded emitter follower circuit of Fig. 4(c) by General Electric Co, U.S.A. This employs bootstrapping of all three shunt elements. C_1 and C_2 values depend on the lowest frequency, f_0, to be passed by the amplifier and can be selected at the nearest preferred values to $C_1 = 1/(150f_0)$ and $C_2 = 1/(50f_{0\mu})$.

Adding a third stage, as for example in Fig. 4(d), makes input impedances in the 100MΩ range possible. With the capacitor values shown, the measured input impedance was about 300MΩ for $f = 0.5$ to 2kHz.

About the limit you can ordinarily push bipolar transistor circuits up to is 1,000MΩ input resistance, although circuits up to $8 \times 10^{11}\,\Omega$ have been constructed. For example, G. W. Horn in "Feedback reduces bio probe's input capacitance" in *Electronics,* March 18, 1968, pp. 97-98, describes a circuit to give 20,000MΩ input resistance shunted by only 0.02pF. A less ambitious example with only 1,000MΩ input resistance is given in Fig. 4(e) to illustrate the various bootstrapping techniques used. The approximate value of the input resistance is $h_{fe1} h_{fe2} h_{fe3} h_{fe4} R$, where R is the parallel combination of the 1.5kΩ emitter resistance of Tr_3 and the amplifier load resistance. Values of $R_{in} = 1{,}000$MΩ at 10Hz and above were obtained dropping to 50MΩ at 1.5 Hz.

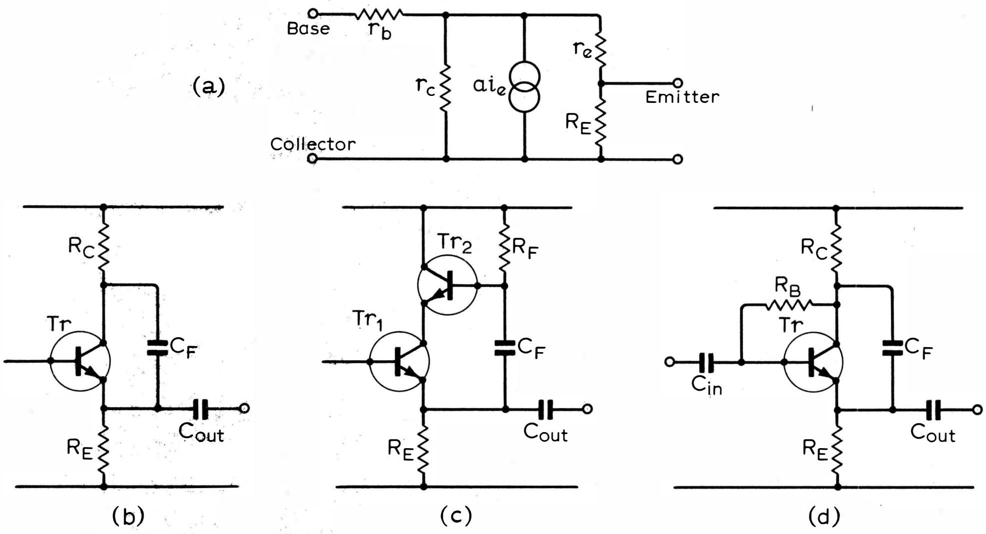
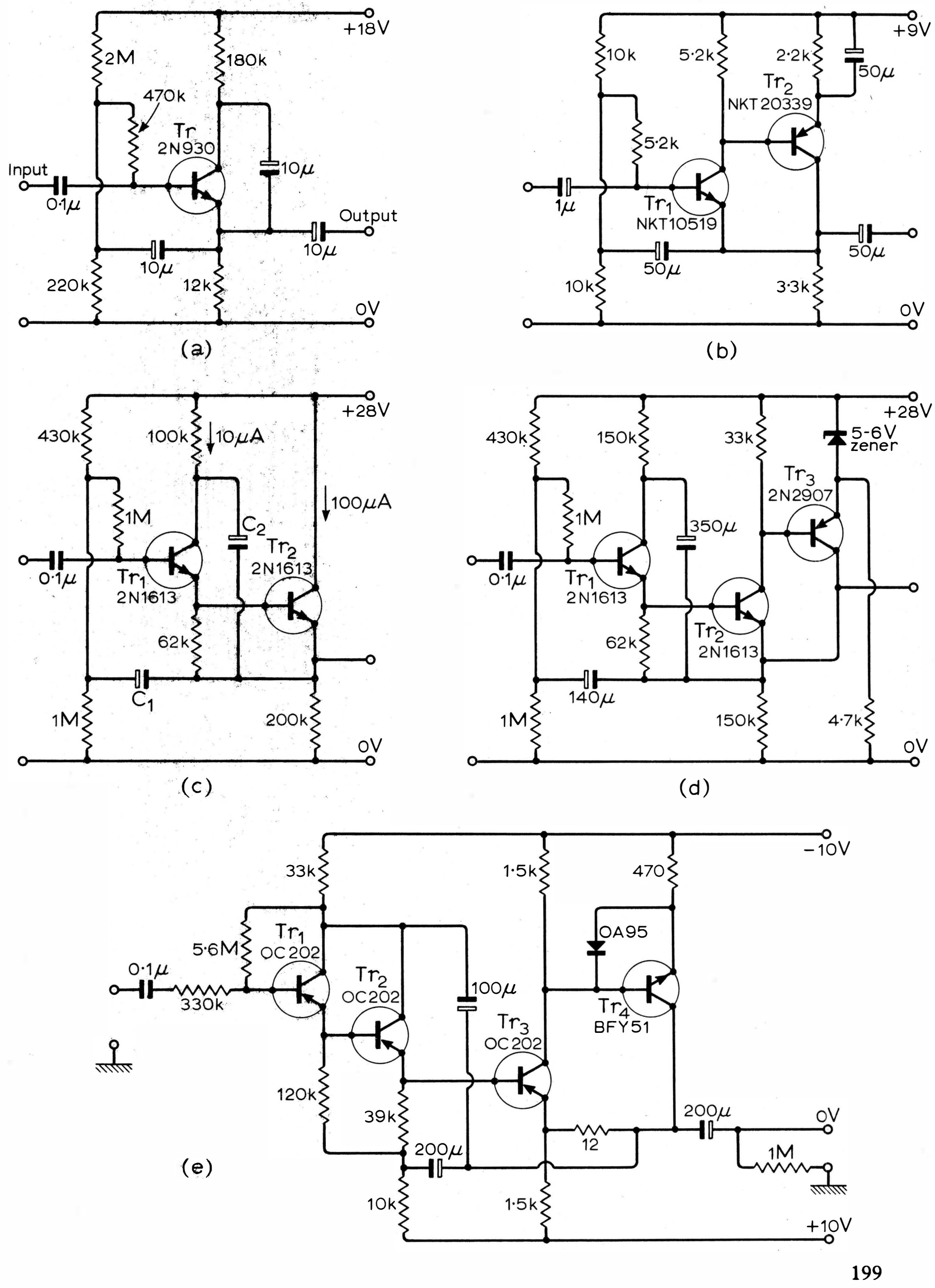


Fig. 3. Reducing shunting of transistor collector output resistance on input impedance. (a) T-equivalent circuit of common collector transistor with external emitter resistor, R_E. (b) Bootstrapping r_c via capacitor from emitter. (c) Bootstrapping r_c via buffer transistor. (d) Simultaneous bootstrapping of r_c and R_B.

Fig. 4. High-input-impedance amplifiers. (a) Single-transistor amplifier with R_{in} greater than 0.5MΩ down to 50 Hz. (b) Two-stage amplifier with 1.5MΩ input and 30Ω output resistances. (c) Two-stage 10MΩ circuit with bootstrapping of all three shunt circuits. (d) Three-stage 300MΩ circuit with bandwidth 0.5 Hz-2,000 Hz. (e) Four-stage 1,000MΩ circuit down to 10 Hz.



F.E.T. high input-impedance amplifiers

The bipolar transistor has a low inherent input resistance (1 - 50kΩ) and we have seen that amplifier input impedances above 1MΩ can be obtained only with quite complex transistor circuits. The f.e.t. on the other hand has a high inhereent input resistance (from $10^9\,\Omega$ upwards with modern devices). Consequently, only simple f.e.t. amplifier circuits are needed to get input impedances at a.f. from 10 to 1,000MΩ, while more complex circuits can

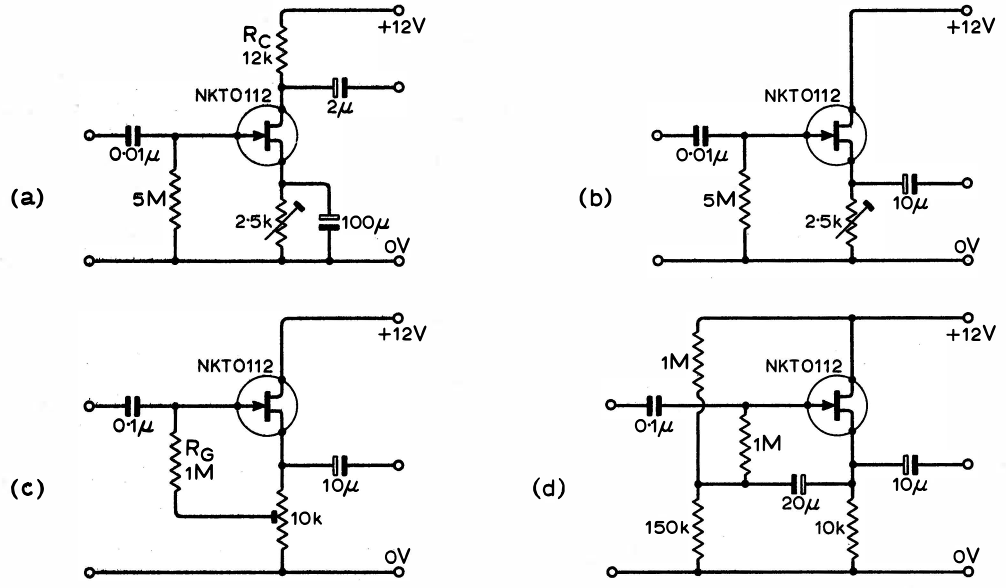


Fig. 5. Single-stage f.e.t. high-input-impedance amplifiers. (a) Common-source amplifier with input impedance of 5M Ω shunted by 30pF. (b) Common-drain amplifier with input impedance of 5M Ω shunted by 2pF. (c) Common-drain temperature-stable amplifier with 15M Ω, 5pF input impedance. (d) Capacitor-bootstrapped amplifier with input impedance of 5M Ω, 3pF.

easily give up to 1,000,000MΩ. The bootstrapping techniques described earlier for bipolar transistors apply equally to f.e.ts, whether p- or n-channel, junction- or insulated-gate, depletion- or enhancement-mode types. The n-channel, depletion, junction f.e.t. is the commonest in use at the time of writing, and most circuitry will be illustrated in terms of this.

Single stage f.e.t. high input impedance circuits: If you want an input impedance of only a few megohms, you can use an n-channel depletion f.e.t. in the common source arrangement for which a typical circuit is given in Fig. 5(a). The NKT0112 here has a typical V_P=1.0V, I_{DSS}=1mA, and g_{mo}=1.5mA/V, and is set up at a bias current of 0.5mA, giving a voltage gain of about 15 times with an a.f. input impedance of 5MΩ shunted by about 30pF.

In the common-drain or source-follower circuit of Fig. 5(b), while the input resistance is still only 5MΩ, the shunt capacitance has been reduces to about 2pF at the expense of voltage gain, $A_v=g_mR_s/(1+g_mR_s)$ which has been reduced to 0.7 times. The 5M Ω input-resistance-controlling gate bias resistor can be increased to 10 or even 15MΩ, but gate leakage currents then make the circuit sensitive to temperature.

The source-follower circuit of Fig. 5(c) with the gate-bias resistor bootstrapped gives high input impedance with better high-temperature stability, because the gate resistor network has a relatively low d.c. resistance. With R_G at 1MΩ as shown in the diagram, Z_{in} is 15MΩ shunted by C_{in}=5pF. Increasing R_G to 10MΩ raises R_{in} to 150MΩ without affecting C_{in}, but the circuit becomes temperature sensitive.

An alternative arrangement sometimes used is shown in Fig. 5(d), where the 20μF capacitor bootstraps the 1MΩ gate bias resistor to give an overall input impedance of approximately 5MΩ shunted by 3pF.

Multistage f.e.t. high input-impedance amplifiers: For better temperature stability and lower input shunt capacitance, the input f.e.t. can be cascaded with bipolar transistor stages, using also bootstrap feedback techniques.

An input resistance of 150MΩ shunted by 5pF is obtained with the circuit of Fig 6(a), which utilizes a common-source f.e.t., Tr_1, *RC*-coupled to a common-emitter transistor, Tr_2, with overall feedback from transistor Tr_2 collector to f.e.t. source to provide the necessary bootstrapping to reduce the shunting effect of the 50MΩ gate bias resistance across the input. With a voltage gain of 26dB, the amplifier has a bandwidth down to 10Hz for any signal source resistance. The top end

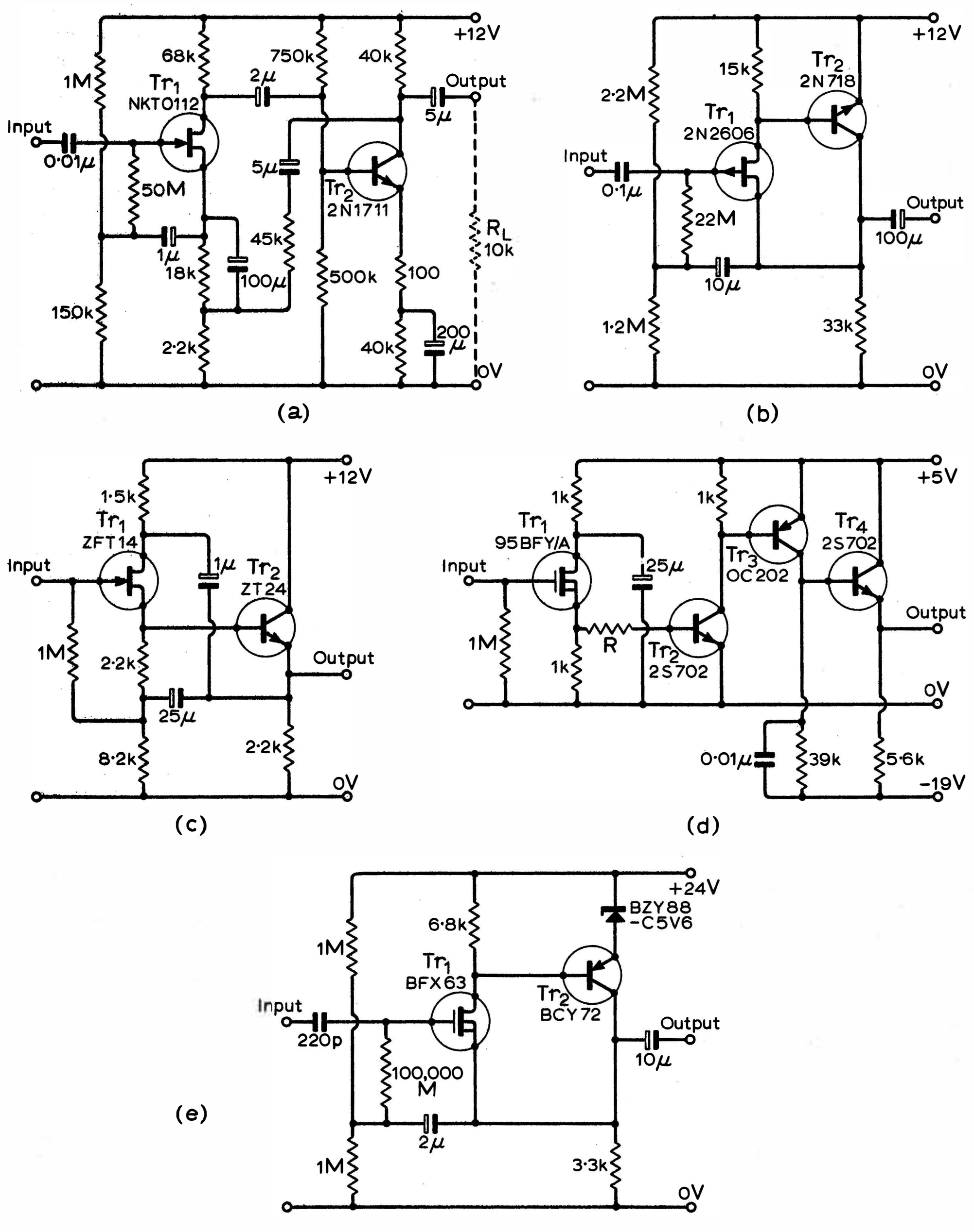


Fig. 6. Multi-stage f.e.t. high-input-impedance amplifiers. (a) 150MΩ, 5pF input impedance with RC-coupled f.e.t. and bipolar transistor. (b) 1,200MΩ, 3.5pF input impedance with d.c.-coupled f.e.t. and transistor. (c) Low input capacitance (0.4pF), high impedance (5MΩ) d.c.-coupled f.e.t. and transistor. (d) 1,000MΩ, 0.1pF input impedance four-stage m.o.s.f.e.t biological amplifier. (e) 1,000,000MΩ input impedance m.o.s.f.e.t. amplifier.

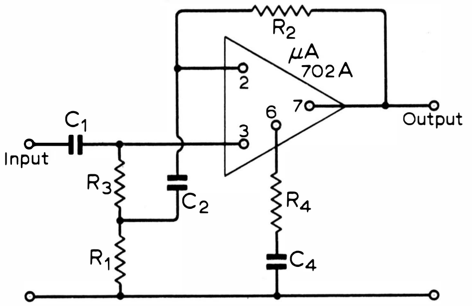


Fig. 7. Connecting up an integrated circuit monolithic operational amplifier to give high input resistance (2-6MΩ).

of the bandpass ranges from 500Hz for a 10MΩ source up to 50kHz for a 10kΩ source.

The Siliconix circuit of Fig. 6(b) shows a p-channel f.e.t. d.c.-coupled to a bipolar transistor to give $Z_{in} = 1{,}200\text{M}\Omega$ shunted by 3.5pF, with an overall voltage gain of 0.98, and an output resistance of 600Ω. Here both the gate bias resistor and the source resistor are bootstrapped.

An input impedance of 5MΩ shunted only by 0.4pF is provided by the d.c.-coupled f.e.t./bipolar pair in the Ferranti circuit of Fig. 6(c). It features overall bootstrapping of both the gate bias resistor and the gate-drain capacitance to achieve the low input shunt capacitance.

The four-stage circuit of Fig. 6(d) given by R. E. Webb in "Field Effect Transistor for Biological Amplifier" in *Electronic Engineering*, December, 1965, pp. 803-805, produces an input impedance greater than 1,000MΩ with a shunt capacitance less than 0.1pF. Using an n-channel depletion mosfet with a gate leakage current of less than 10^{-11} A, it features unity voltage gain with an output resistance of only 25Ω. The amplifier and input connections have to be doubly screened. The internal screen is connected to the amplifier output and the external screen to ground, thus reducing the stray capacitance to ground by the same amount as the input resistance is increased by the large overall feedback from the top of the 5.6kΩ last emitter load resistance.

As the final f.e.t. example, the relatively simple Mullard circuit of Fig. 6(e) gives an input resistance of 1,000,000MΩ with a voltage gain of about 0.98 and an output resistance of only 50Ω. The f.e.t. 3.3kΩ source resistor is bootstrapped by the BCY72 transistor, as is also the $10^{11}\Omega$ gate bias resistor via the 2μF capacitor.

High input impedance with i.c. operational amplifier

Engineers are now beginning to use integrated circuit monolithic operational amplifiers as complete circuit elements instead of building up circuits with discrete bipolar transistors or f.e.ts. High input impedance can be obtained with these by the simple expedient of putting the required input resistance in series with the amplifier input, which is a virtual earth point. However, bootstrapping techniques can also be used as shown in Fig. 7. Here a standard Fairchild μA702A operational amplifier is set up for positive feedback from the output to the non-inverting input pin (3). The approximate expression for the overall low frequency input impedance is $R_{in} = A_{vo}R_A/A_f$, where A_{vo} is the open loop voltage gain, A_f is the gain with feedback and R_A is the input impedance into pin (3). By general operational amplifier theory, A_f can be shown to be approximately $(R_1 + R_2)/R_1$. For the μA702A, typically $A_{vo} = 2{,}000$, and $R_A = 10\text{k}\Omega$. Two sets of circuit component values are given below to produce input resistances of 2 and 6MΩ.

C_1	C_2	C_4	R_1	R_2
1μF	1μF	910pF	10kΩ	91kΩ
1μF	4.7μF	1000pF	51kΩ	100kΩ

R_3	R_4	A_v	R_{in}
82kΩ	220kΩ	10	2MΩ
51kΩ		3	6MΩ

The phase-shift network, R_4, C_4, provides frequency stability. For best thermal stability, $R_1 + R_3$ should be made equal to R_2.

When f.e.t.-input operational amplifiers become commonly available, they will have an input terminal resistance, R_A, of the order of 10MΩ. Looking back at the formula for bootstrapped input resistance given for the bipolar μA702A, it will be seen that very high overall input resistances can be expected in the future with f.e.t. operational amplifiers.

Announcements

The series of Philips **colour television courses** for service engineers, started in July 1967 by Combined Electronic Services Ltd, have ceased for the time being. Over 1,000 people attended. Plans are now under way for a new series scheduled for the Autumn. The courses will be of 4 days' duration and take place at the colour television school at C.E.S. Ltd, Waddon, Croydon, Surrey.

A one-day symposium on "The Numerical Solution of Laplace's Equation" will be held at the John Dalton College of Technology, Chester Street, Manchester 1, on 8th July. Fee £4 15s.

At the recent annual general meeting of the **Radio & Electronic Component Manufacturers' Federation,** the following result of the postal ballot for the election of the Council was announced:— Belling & Lee (N. D. Bryce), A. F. Bulgin & Co. (R. A. Bulgin), Colvern (R. F. Collinson), A. H. Hunt (S. H. Brewell), McMurdo Instrument Co. (F. W. Irons), Mullard (Dr. F. E. Jones, elected chairman), Multicore Solders (R. Arbib), Painton & Co. (C. M. Benham), and Standard Telephones & Cables (E. E. Bivand).

The **Institution of Electrical and Electronics Technician Engineers** has decided to accept the City and Guilds of London Institute's Electrical Technicians' Certificate with two endorsement certificates as satisfying the technical education requirements for election to the class of Graduate.

The Munich Fair and Exhibition Co. have announced that the fourth **Electronica**—the international trade exhibition of electronic components and related measuring and production equipment—will be held from 22nd to 28th October, 1970. The third Electronica exhibition takes place this year from 7th to 13th November.

An agreement has been reached, subject to contract, between **Rediffusion Ltd** and the **Rank Organisation Ltd,** for the purchase by Rediffusion of the whole of Rank's wired sound and television networks and the television set rental business associated with these relay undertakings.

Industrial Instruments Ltd, the Bromley, Kent, manufacturers of Transipack inverters, have been appointed U.K. agents for Varo-Atlas, the American company whose interests lie in the military static inverter field.

The Venner Group have recently announced an agreement with **Control Logic Inc.,** of Massachusetts, which gives Venner manufacturing and sales rights for a family of integrated circuit logic cards and accessories. This agreement applies exclusively in the U.K., the Commonwealth and all E.F.T.A. countries.

S. Davall & Son Ltd, of 4 Wadsworth Road, Greenford, Middlesex, have appointed **agents in France and North America** for the precision relays and associated components made by their manufacturing division, Perivale Controls Co. Ltd. The agents are Crouzet S.A., of Paris, for Common Market countries and Eastern Electric Company, of Montreal, for Canada and the United States.

Standard Telephones & Cables Ltd, have been awarded a contract by Hawker Siddeley Aviation, worth approximately £250,000, to supply **aerial systems** for the Hawker Harrier V/STOL aircraft destined for service with the R.A.F.

A £430,000 contract has been placed with the M.E.L. Equipment Company Ltd, by the Ministry of Technology on behalf of the Ministry of Defence (Army Department), for the supply of **military radio equipment.** The equipment comprises single sideband h.f. transmitters L.556 and radio telegraph adaptors L.607.

Racal Communications Ltd, of Western Road, Bracknell, Berks., have received contracts to the value of £1M for new **submarine h.f. communication equipment** for use by the Royal Navy.

An order worth approximately £400,000 has been awarded to Standard Telephones and Cables Ltd, by the Italian Ministry of Defence, for **instrument landing systems** to be installed at the airports of Rome, Turin, Milan, Genoa, Venice and Naples.

Cossor Electronics Ltd, of Harlow, Essex, have received an order, worth approximately £250,000, for the supply and installation, at Stornoway, Isle of Lewis, and Burrington, Devon, of two dual-channel and two single-channel SSR 700 interrogator systems.

Henry's Radio Ltd, have opened an additional electronics centre at 309 Edgware Road, London W.2.

A licensing agreement has been completed between the Decca Navigator Company, London, and International Standard Electric Corporation, a subsidiary of International Telephone and Telegraph of U.S.A., to co-operate in the field of marine and commercial aviation electronics.

Thorn Electrical Industries (London) and International Rectifier Corporation (California) have signed a 12-year agreement to continue as **joint ventures** the six jointly owned semiconductor companies in Europe. International Rectifiers will exercise management control (receiving a management fee) and will provide technical assistance and licences relating to semiconductor products.

Texas Instruments and Sony announced that the Japanese Government has approved the establishment of **Texas Instruments Japan Ltd.** Fifty per cent of the capital is to be furnished by each of the companies, and semiconductor devices including integrated circuits and certain electrical control devices are to be manufactured.

Amphenol and Plessey recently signed an agreement whereby the new Astro 348 connector range developed by the Amphenol Corporation of Illinois is to be manufactured by the Plessey Company Ltd.

GEC-AEI Telecommunications Ltd. of Coventry, have won orders worth £250,000 for completely solid state 2 GHz and 7 GHz radio links and multiplex equipment in Hong Kong and Bahrain. The contracts have been placed by Cable and Wireless Ltd.

Marconi Company, of Chelmsford, have won a contract valued at £700,000 to supply a completely new television system to the state of Bahia in Brazil.