Mains rejection tracking filter

Using a tracking "n-path" filter with wide dynamic range

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The filter described greatly reduces interference at mains frequency and harmonics on wideband signals without seriously affecting these signals. It has the ability to track changes in the mains frequency, enabling very sharp rejection characteristics to be obtained. Useful rejection is maintained up to the 5th harmonic. The filter is based on the well-known principles of the commutating *CR* network but several improvements have been made to extend the dynamic range of this network without sacrificing signal bandwidth. For example, at mains fundamental a rejection greater than 40dB is maintained down to signal levels of 50mV r.m.s., the signal bandwidth being 100kHz. Consider the situation in which *N* identical capacitors are switched into a *C*-*R* network in sequence at a rate of Nf_o Hz (Fig.1).

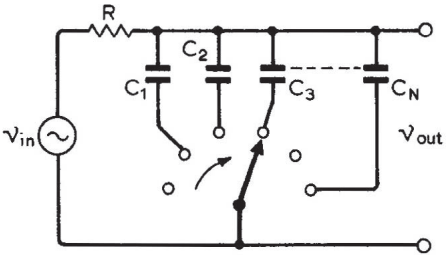


Fig. 1

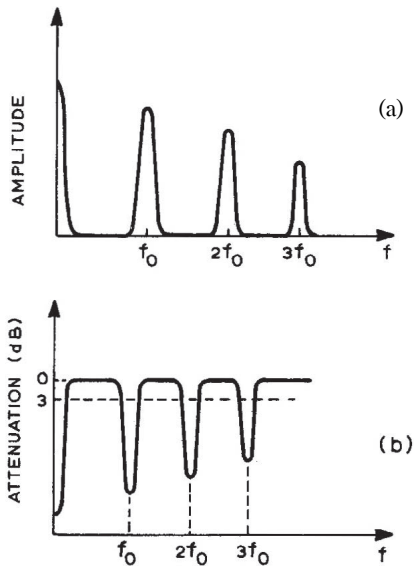


Fig. 2

The transfer characteristic of the network has the form indicated by Fig. 2(a), i.e. the network acts as a comb filter, the centre frequencies of which are set by the commutating frequency of the switch.[1] Alternatively, if the output is taken across the resistor the transfer characteristic of Fig. 2(b) is obtained.

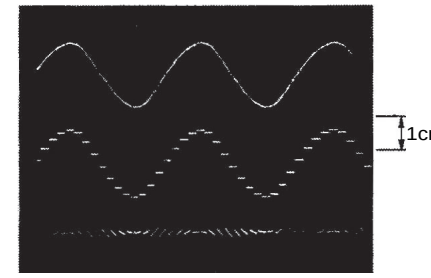
If the commutating frequency, Nf_o, is controlled to follow variations in f_o, the filter has the ability to track varying-frequency input signals therefore enabling the use of sharp notches while maintaining high attenuation. This is in contrast to fixed-frequency notch filters such as the bridged-T network. Although the mathematical treatment of commutating filters is well established it is useful to describe their operation in a non-mathematical way for the purpose of discussing problems which arise in the design of an instrument.

Principle of operation

Suppose the input signal v_{in} in Fig. 1 is sinusoidal at a frequency *f*Hz. If *f* is equal to nf_o, where *n* is an integer, the input signal will be in synchronism with the switch and each individual capacitor will be switched in at the same instant in each cycle of the input waveform. Each capacitor will charge up to the corresponding instantaneous value of the input waveform. This is analagous to sampling the input waveform with *N*/*n* samples per cycle. Obviously the upper limit on n is N/2.

The voltage waveform across *C* will not be sinusoidal but will resemble a "staircase" replica of the sinusoidal input voltage. The voltage across *R* will be the difference between the sine-wave and the staircase waveform. Consequently the action of the filter necessarily introduces high-frequency switching noise. An illustration of this noise is shown in the photograph of Fig. 3, which was taken for the case with f_o = 50Hz, n = I, N = 16.

Consider now the action of the filter if *f* is a non-integral value of f_o. The input is no longer in synchronism with the switch and each individual capacitor will be switched in at varying points in successive cycles of the input waveform. The voltage across each capacitor will therefore be averaged to zero and the voltage across R will be equal to the input voltage. At input signal frequencies very much lower than f_o the



vert 0.5V/cm.
horiz, 5m sec./cm.

Fig. 3

switch may be considered to be rotating so rapidly that all *N* capacitors appear to be connected simultaneously. The circuit can then be thought of as a simple network with a time constant of *NCR* i.e. the voltage across *R* is down by 3dB at a frequency $1/2\pi NCR$ Hz. At input frequencies much higher than f_o the switch may be considered stationary and the network thought of as a simple network with a time constant of *CR*. This usually means that the voltage across *C* is very much smaller than the input voltage at frequencies greater than $Nf_o/2$ even though the commutation is no longer effective. Hence the voltage across *R* will be almost equal to the input voltage. The switching has the effect of reflecting the loss-pass response about f_o, $2f_o$, etc, thereby generating the comb-filter response of Fig. 2(a). The bandwidth is $2/N$ times the bandwidth of the original low-pass sections, i.e. $(2/N)(1/2\pi CR) = 1/\pi NCR$.

Design considerations

The desirable characteristics of a tracking mains interference rejection filter may be summarized as follows.

1. Minimum degradation of the signal which is to be transmitted through the filter.
2. Wide dynamic range and signal bandwidth.
3. High rejection of the fundamental and lower harmonics of the mains frequencies bearing in mind that interference signals are liable to fluctuate in amplitude.
4. Ability to track changes and rates of change of the nominal mains frequency.

As point 4 is subsidiary to the operation of the filter it is considered briefly before proceeding to a more detailed discussion of points 1, 2 & 3.

Tracking requirements

Statutory limits of the mains frequency in this country are 49.5Hz and 50.5Hz, although the likelihood of these limits being reached is low under normal circumstances. The rate of change of mains frequency is governed by the inertia of the generating plant and it is extremely unlikely that a rate of change of 0.1 Hz/min. would be exceeded. The tracking requirements are modest therefore and the circuit described later has an adequate performance.

Rejection, signal bandwidth and dynamic range

A convenient way in which to discuss the performance of the filter is to consider the various properties of the basic circuit and then discuss how these properties may be improved. The basic filter, omitting the tracking loop, is shown in Fig. 4.

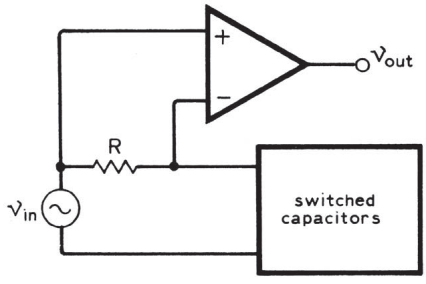


Fig. 4

Considering firstly the rejection characteristics of this circuit, as illustrated in Fig. 2(b), the sharpness of rejection is proportional to *NCR*. In theory one can obtain a very high Q-factor by choosing an appropriately large value of *NCR*. But an interference signal is likely to have a fluctuating amplitude. Suppose, for the sake of argument, that a 50-Hz interference signal was fluctuating sinusoidally in amplitudes with a period of ten seconds. Obviously this may be considered as a double-sideband signal with a carrier at 50Hz and sidebands at 50 ± 0.1 Hz. If the Q of the filter at 50Hz were greater than 50/0.2 the sidebands would not be greatly affected. Although the analysis of sinusoidally modulated mains interference is a fictitious case it serves to illustrate that one must not have too high a Q-factor if fluctuating interference signals are to be rejected. Also, the step response of the filter is determined by its Q such that a slow response would result if a very high value of Q were used.

Theoretical magnitudes of rejection obtained at the synchronous frequencies can be found fairly easily by numerical analysis for specific values of *N*. The procedure is explained in the following paragraph.

Consider a sinusoidal input signal of frequency nf_o Hz. In the steady-state condition the voltage across each capacitor will reach the value of the input sine-wave averaged over the period for which the capacitor is connected. The voltage across each capacitor may be assumed constant provided that the *CR* time constant is large compared with the time spent on each capacitor and also if there is negligible discharge of the capacitors during the time between consecutive connections, i.e. $1/f_o$ sec. The waveform

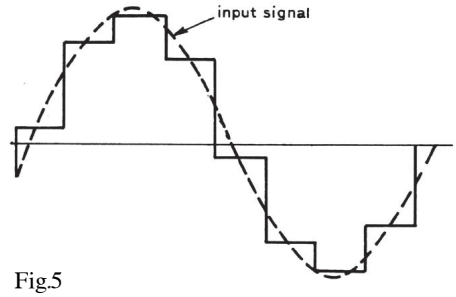


Fig.5

across the capacitors will thus be as illustrated in Fig. 5.

The Fourier analysis of this type of waveform appearing across the capacitors may be found numerically by the "jump" technique.[2] As an example, suppose *N* were equal to 16. The analysis yields the result that for input signals of frequency f_o, $2f_o$ and $3f_o$, the fundamental components of the waveforms across the capacitors are respectively 0.97, 0.95 and 0.905 times the input. This would lead to rejections of 30.4, 26 and 20.4dB respectively if these fundamental components alone were subtracted from the input signal. However, these figures may be improved by weighting one of the inputs of the subtractor. In this way infinite rejection can be achieved at one of the synchronous frequencies, i.e. fo, $2f_o$ or $3f_o$ etc. For example, if the circuit were trimmed to effectively increase the 0.97 figure to 1.00, the theoretical rejections at f_o, $2f_o$ and $3f_o$ would be ∞, 33 and 23dB respectively.

Considering, secondly, the dynamic range of the circuit, it was mentioned previously that the commutating action of the filter introduced high-frequency switching noise. Being more specific, if a 50-Hz signal were present at the input, switching noise would be introduced at $50N + 50$, $50N$, $100N$, $150N$. . . etc, Hz. Furthermore, amplitudes of the switching noise components are at fixed levels below the 50-Hz signal. In general, the switching-noise component amplitudes decrease as *N* increases. As there is obviously a practical limit to the value of *N* the output of the basic filter will contain components of switching noise which will limit the dynamic range of the filter.

The simplest way in which to improve the dynamic range is to add a low-pass filter to the output as shown in Fig. 6, this of course reducing the signal bandwidth. To exploit the rejection properties of the commutating filter this low-pass filter should have negligible attenuation up to say $(N/2)$50Hz and high attenuation at N50Hz. The inevitable choice would be an active *R-C* filter.

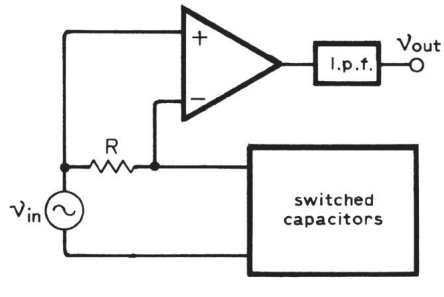


Fig. 6

Good dynamic range and signal bandwidth can be achieved if a low-pass filter is inserted in the position shown in Fig. 7.

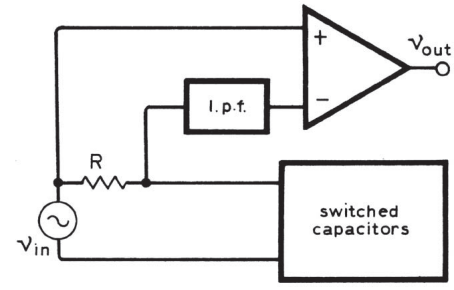


Fig. 7

The low-pass filter must again have a very sharp cut-off but unfortunately this cannot be achieved without introducing phase-shift in the pass-band. As a result the rejection decreases since the interference signals present at the differential amplifier inputs will no longer be exactly in phase.

This disadvantage may be overcome by inserting an all-pass filter in the signal path, having exactly the same phase response as the low-pass filter so that the interference signals present at the inputs of the differential amplifier are now always in phase, resulting in the final block diagram of Fig. 8.

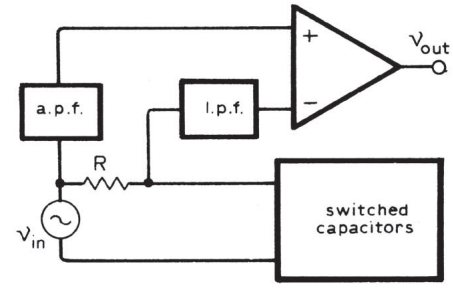


Fig.8

Unfortunately the wanted signal now undergoes the phase-shift of the all-pass filter. This mayor may not be important depending on the application.

To summarize, the filters based on the block diagrams of Figs 6, 7 & 8 have the following properties:

Fig. 6—high rejection, low signal bandwidth, good dynamic range

Fig. 7—high signal bandwidth, good dynamic range, moderate rejection

Fig. 8—high signal bandwidth, high rejection, good dynamic range but unsuitable for applications which require little phase-shift through the filter.

All of these characteristics may be obtained from the constituent parts of Fig. 8 by a suitable switching arrangement, though not simultaneously.

Choice of N and CR

Good rejection and tolerable levels of switching noise without overdue circuit complexity can be achieved with $N = 16$. If a bandwidth of 1Hz at 50Hz is specified, i.e. Q= 50, the filter will have a negligible effect on a wideband signal. Also, with a

half-bandwidth of 0.5Hz reasonable rejection will still result at frequencies between 49.8 and 50.2Hz, i.e. the filter would reject a 50-Hz interference signal even if its amplitude were fluctuating over periods as short as 5s and further with a Q of 50, the time constant of the filter is 0.3s so that a rapid response to step changes in interference level is achieved.

Complete layout

The complete block diagram of a practical mains rejection filter is shown in Fig. 9. A switching arrangement has been adopted to make maximum use of the characteristics of the commutating network.

In position 1 (cf. Fig. 8) there is high signal bandwidth, high mains rejection, good dynamic range but considerable phase-shift between input and output. Position 2 again yields high signal bandwidth and good dynamic range but moderate mains rejection (cf. Fig. 7). However, the phase-shift is now constant over the audio range of frequencies. This is accomplished simply by shorting out the all-pass filter. The effect of the phase shift of the low-pass filter is to reduce the rejection of mains frequencies. However, the 50-Hz rejection is improved by introducing a simple lead network (C_1, R_1)

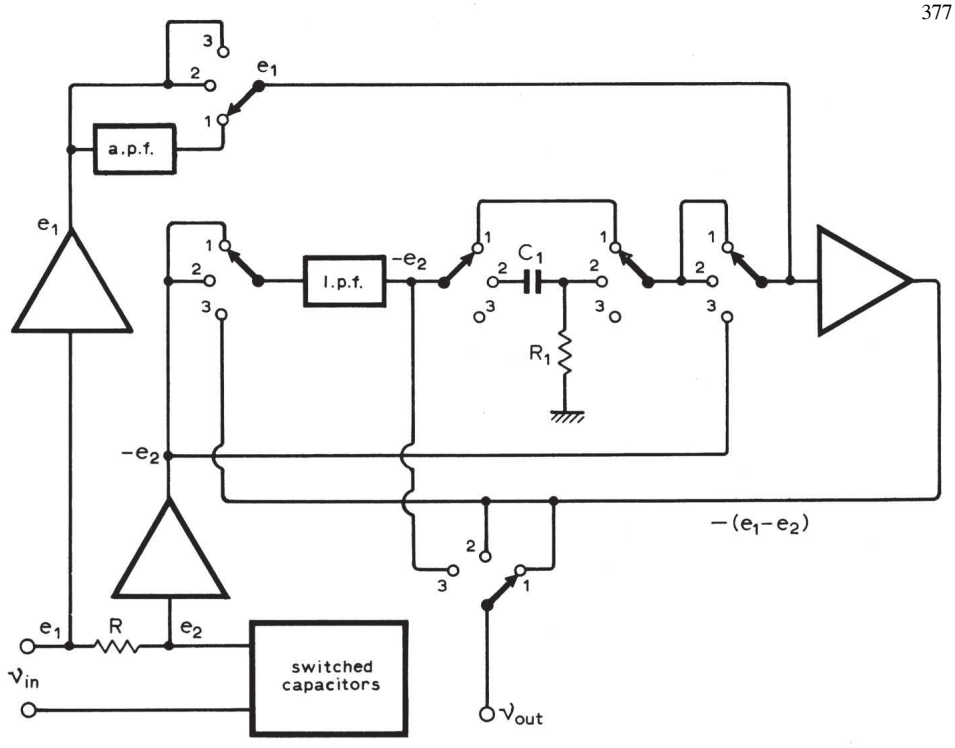


Fig. 9

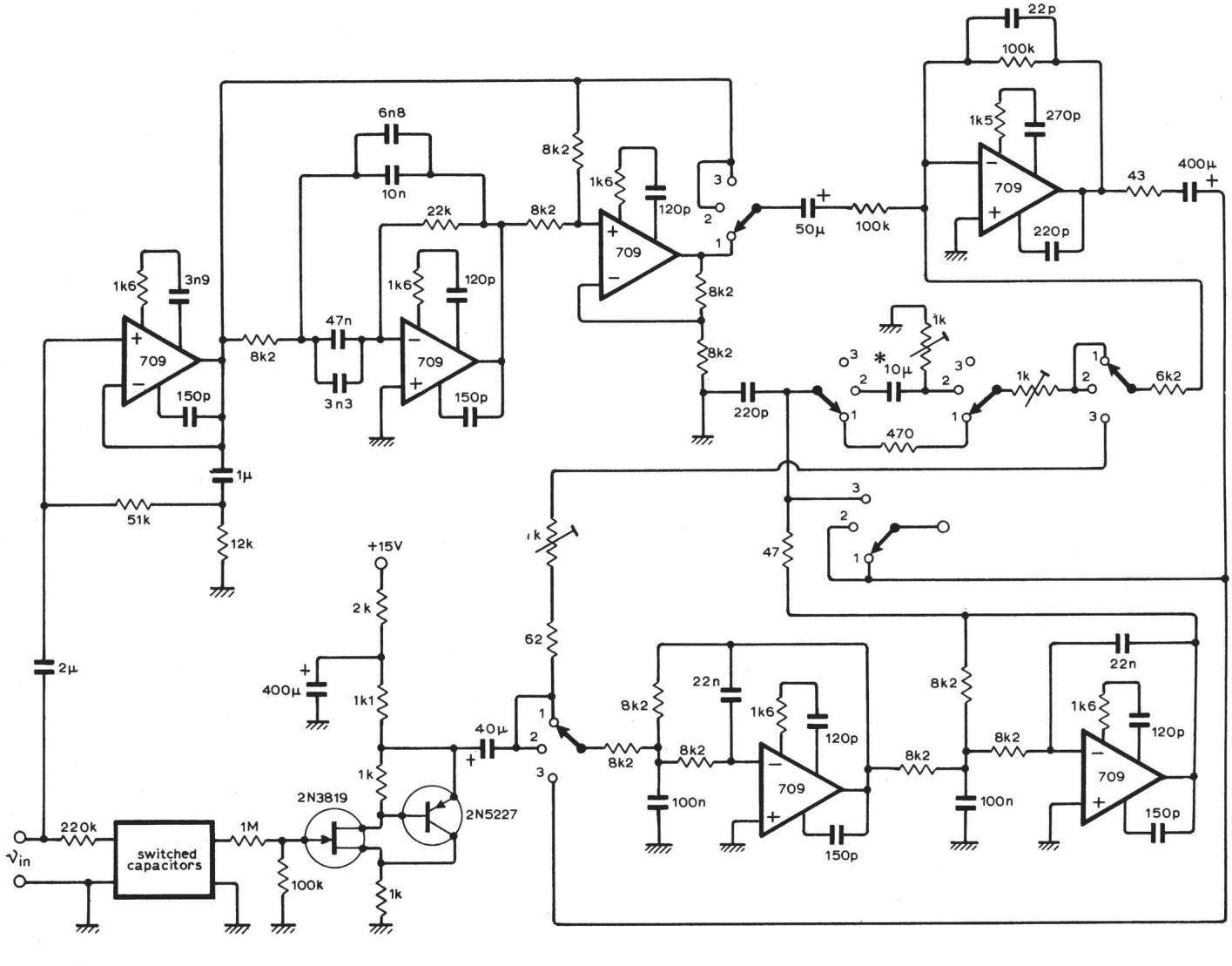


Fig. 10

chosen so that at 50Hz, though not at higher harmonics, the interference signals are exactly in phase at the inputs of the differential amplifier.

Position 3 gives high mains rejection, good dynamic range but low signal bandwidth, determined by the low-pass filter (cf. Fig. 6). This position was found to be desirable in certain applications where high frequency signals cause problems.

The low-pass and all-pass filters are both non-inverting and need to be preceded by buffers. Because an adder is far easier to align than a subtractor with its four variables we made the buffer preceding the all-pass filter a follower and the other an inverter, thus enabling an adder to be used to derive the required difference between the interference signals.

The circuit diagram corresponding to the block diagram of Fig. 9 is shown in Fig. 10.

Commutation

The 16 capacitors must be commutated electronically at 16 X mains frequency. Anyone of a number of methods may be used to this end and the technique chosen is to drive two 8-way multiplexers alternately, both consisting of eight m.o.s.f.e.ts, each of which is switched on in turn with consecutive input clock pulses. The multiplexers are connected thus

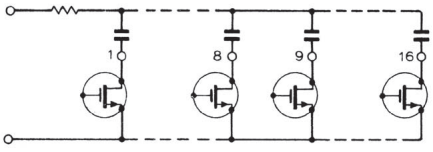


Fig. 11

The f.e.ts 1 to 16 are therefore arranged to switch on in turn. An 800-Hz clock (described later) drives a four-stage binary counter, the output of which is a 50-Hz square wave.

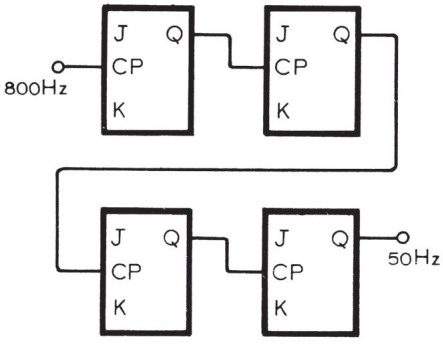


Fig. 12

In Fig. 12 all J and K inputs are permanently high. The 800-Hz clock is used to drive the two multiplexers. Consider just one multiplexer. Each f.e.t. is energized in turn as consecutive clock pulses appear at the input but after eight pulses, the clock waveform must be diverted to the second multiplexer which then switches capacitors 9 to 16 and then back to the first multiplexer, etc.

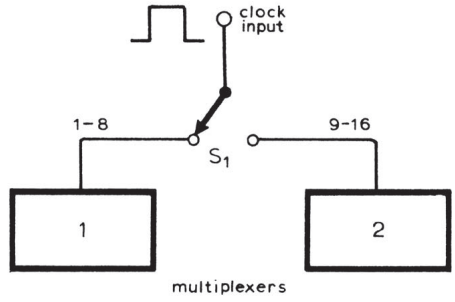


Fig. 13

Referring to Fig. 13, switch S_1 must toggle every eighth clock pulse. Now the output of the counter of Fig. 12 toggles every eighth clock pulse and so switch S_1 may be simulated as follows

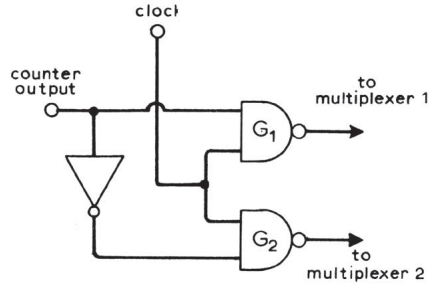


Fig. 14

When the counter output is high, gate G_1 is enabled and its output will then consist of the 800-Hz clock waveform. Meanwhile G_2 is closed. After eight clock pulses the counter output assumes a low state and gate G_2 is now enabled while G_1 closes.

Tracking oscillator

A multivibrator with a pulse repetition rate of $N \times$ mains frequency will provide the clock waveform. If the mains frequency changes slightly, then so must the multivibrator repetition rate to maintain synchronism.

Consider the following circuit

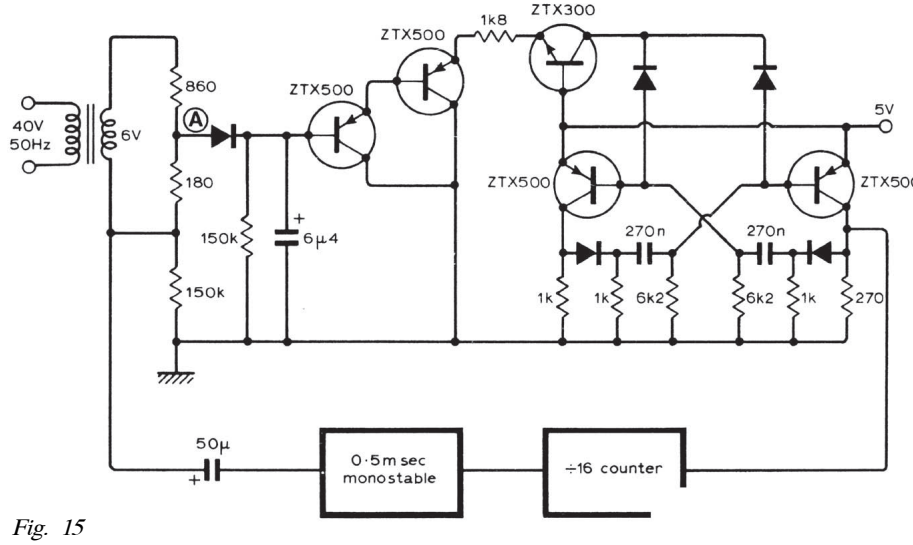


Fig. 15

The waveform at point A will be a 50-Hz sinewave with a pulse superposed on it:

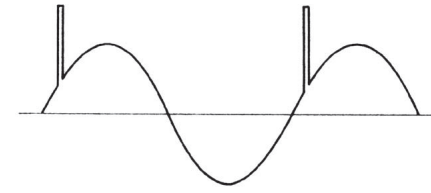


Fig. 16

When the multivibrator is synchronized to the mains frequency, the 0.5ms pulse will sit on the sinewave at some particular point. If the mains frequency now changes slightly, the pulse will climb up or slide down the sinewave and if the peak value of the waveform of Fig. 16 is detected, the resulting voltage can be used to vary the multivibrator rate to maintain synchronism with the mains.

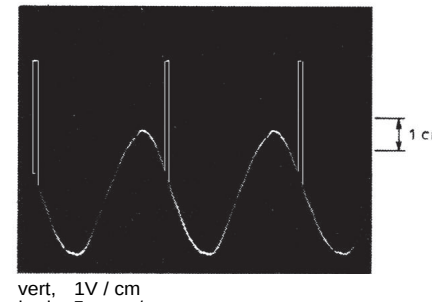


Fig. 17

Fig. 17 shows a photograph of the waveform at point A. The monostable of Fig. 15 is based on that given in reference 4.

A graph of p.r.r. versus mains frequency is shown below

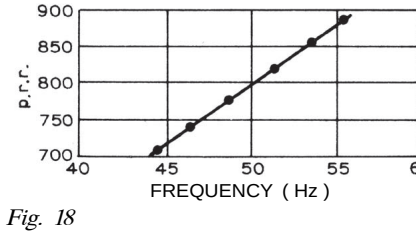


Fig. 18

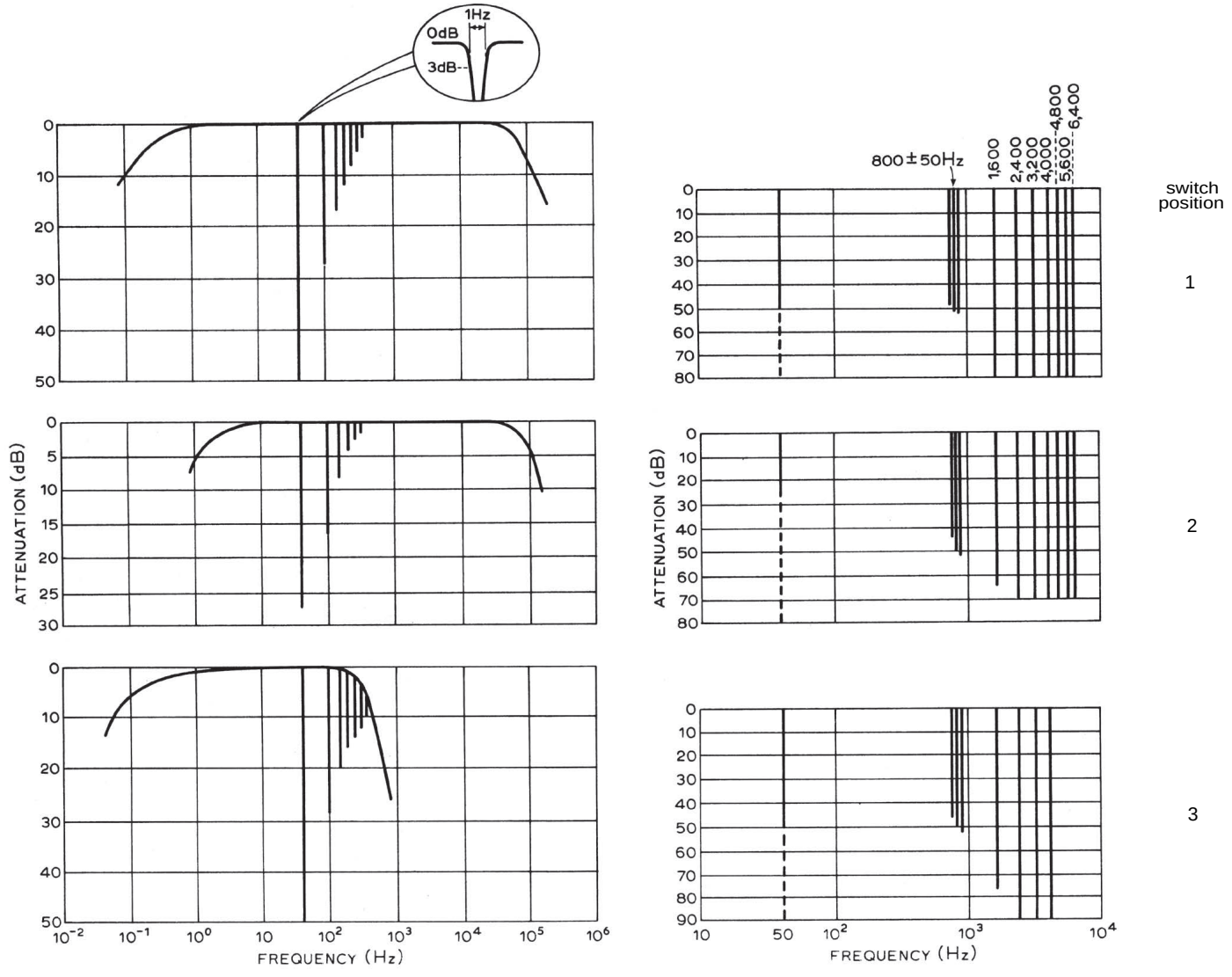


Fig. 19

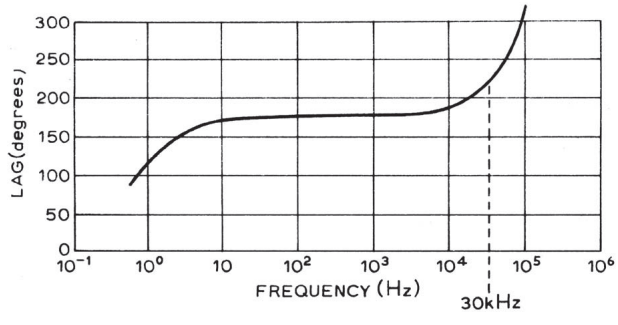


Fig.20

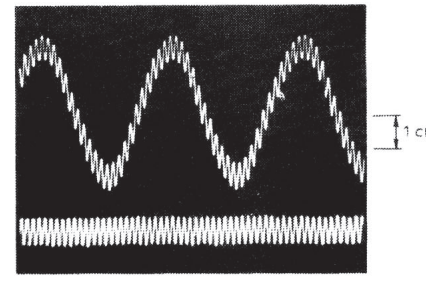


Fig. 21

Performance

In position 1 (see Fig. 19, top left), 50dB of rejection at 50Hz was maintained down to 100mV and up to 2V rms and 40dB of rejection down to 50mV. A bandwidth of 100kHz was maintained up to levels at which the slew rate of the operational amplifiers employed (709s) imposed restrictions.

The graphs on the right-hand side of Fig. 19 illustrate the relative amplitudes at the output terminals of an unwanted 50-Hz signal and its associated switching components, the input 50-Hz signal level being 0dB.

In position 2, 27dB of rejection was achieved at 50Hz, again from 100mV to 2V r.m.s. Phase response is shown flat from 2Hz to 30kHz in Fig. 20.

In position 3, 50dB of attenuation was measured between 100mV and 2V r.m.s.

The 3-dB bandwidth of all the notches of the left-hand graphs was approximately 1Hz.

Fig. 21 illustrates the effectiveness of the filter where the top trace shows a 1-kHz sinewave swamped by 50Hz and the lower trace displays the 1-kHz signal after being processed by the filter.

References

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