MICRO-CONTROLLED RADIO-CODE CLOCK

Several standard-frequency transmissions throughout the world provide time and date information controlled by caesium atomic clocks, with potential for automatic time and date information at reasonable cost. This design offers a compromise between economy and complexity suitable for both non-critical professional applications and domestic use.

by N. E. Sand

The 60kHz standard-frequency transmission from Rugby MSF now includes fast and slow time codes, both of which provide full time and date information once every second. The signal is transmitted 24 hours every day except for a maintenance period on the first Tuesday of each month. The transmitter power is 50kW e.r.p. which, with the long wavelength, provides propagation over a range of several hundred miles. With careful circuit design, useable reception can be achieved throughout Britain, but because there is a skywave and groundwave component, certain areas can experience cancellation or addition where mixing takes place. This problem is complicated because the areas of mixing change from daytime to nightime as the ionosphere changes.

Successful reception has been achieved with specialized equipment at over 3,000 km from the transmitter, but with simpler designs 750 km is a more realistic range.

This design uses the slow code, which for most applications provides better results and requires less critical timing. The slow code format shown in Fig. 1 extends from second 17 to second 59 each minute. A logic zero is represented by a carrier break of 100ms and a 1 is represented by a break of 200ms. Other information, such as parity bits, is represented by a carrier break of 100ms displaced by 200ms from the start of the second. To synchronize with the serial code it is necessary to recognize the start of each minute, so an identifier sequence from second 52 to 59 is provided.

***Fig. 1.** Slow-code format from Rugby MSF.*

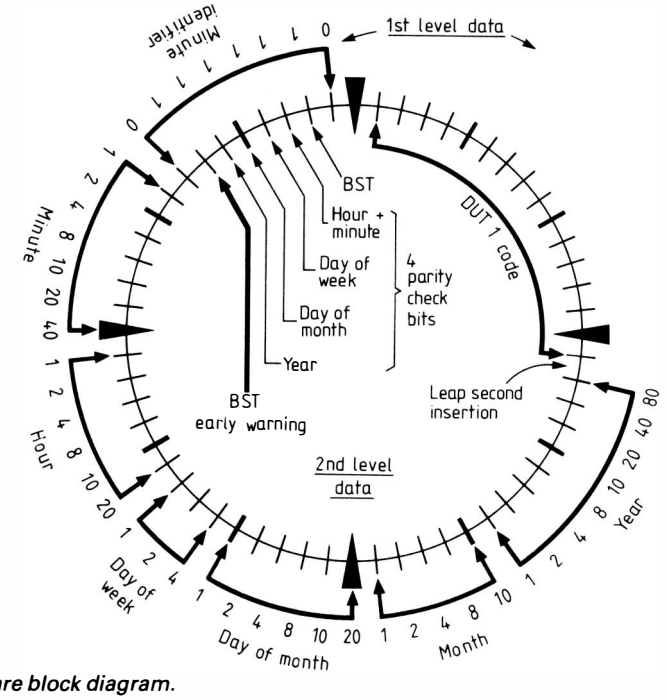
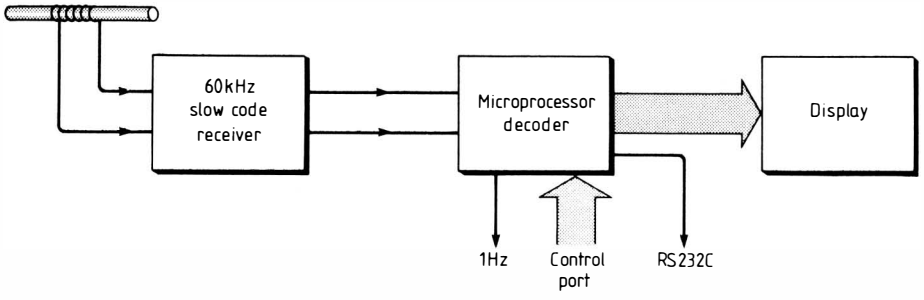


***Fig. 2.** Hardware block diagram.*



The most important part of the design, as shown in Fig. 2, is the receiver which must be capable of producing a consistent output in the presence of noise. Unfortunately there are several common sources of interference at 60kHz, for example the harmonics from the line output transformer of colour television receivers are powerful sources of interference for v.l.f. transmissions, as well as fluorescent tube fittings and even hand-held calculators. Carefully designed t.r.f. and phase-locked loop receivers can work satisfactorily at moderate gains, but commonly suffer from self pick up which limits their sensitivity. In the case of the p.l.l., radiation from the v.c.o. will generally weaken the signals. For best results a low-current superheterodyne receiver should be used, but it is costly and difficult to adjust for optimum noise performance at v.l.f.

An alternative receiver which is much simpler and with careful design can produce acceptable results is shown in Fig. 3. The input stage uses a cascode circuit which enables the antenna coil to be directly connected without a transformer winding and gives good stability at high gain by minimizing Miller feedback. A multiplier* is used for low-level detection of the 60kHz carrier, a technique which avoids high levels of 60kHz and therefore enhances receiver stability. The multiplier generates a double frequency component and a differential voltage proportional to the carrier level at the two load resistors. The double frequency output is ignored by the following amplifier stage which produces the demodulation carrier. To minimize power requirement, operating current in each arm of the multiplier is set to 50μA. To avoid drift at the multiplier output the potentiometer should be a ten-turn cermet type and the two load resistors metal film.

To optimize receiver performance for all signal levels at the antenna a normal gain-control loop to the cascode stage would provide satisfactory results. However, a better method is to gate the a.g.c. loop because the 60kHz carrier is 100% modulated and will cause errors in a conventional loop. In this design an undelayed signal from the output of IC_2 switches the

* Self-setting time code clock, by N. C. Helsby, *Wireless World*, August 1976, pp?

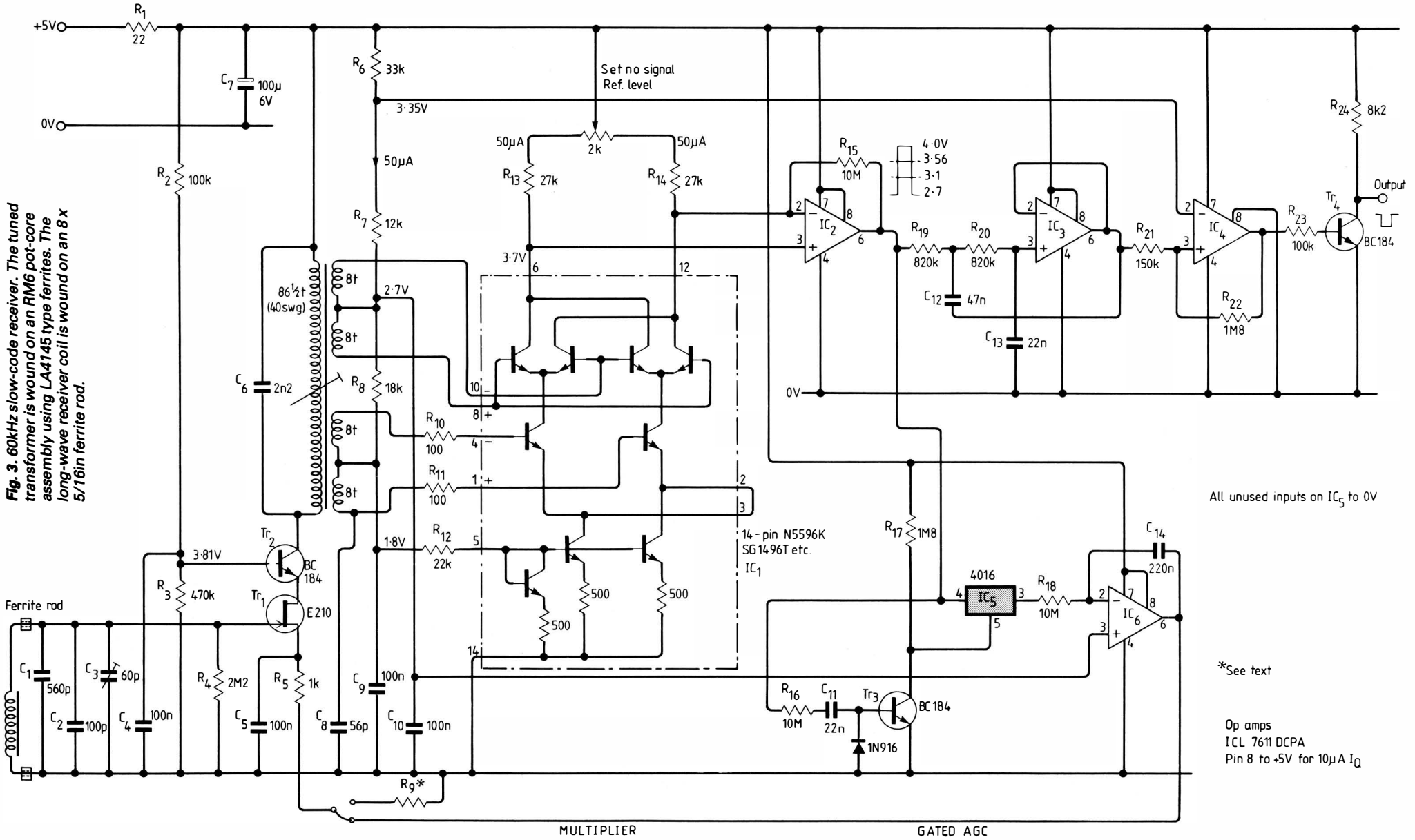
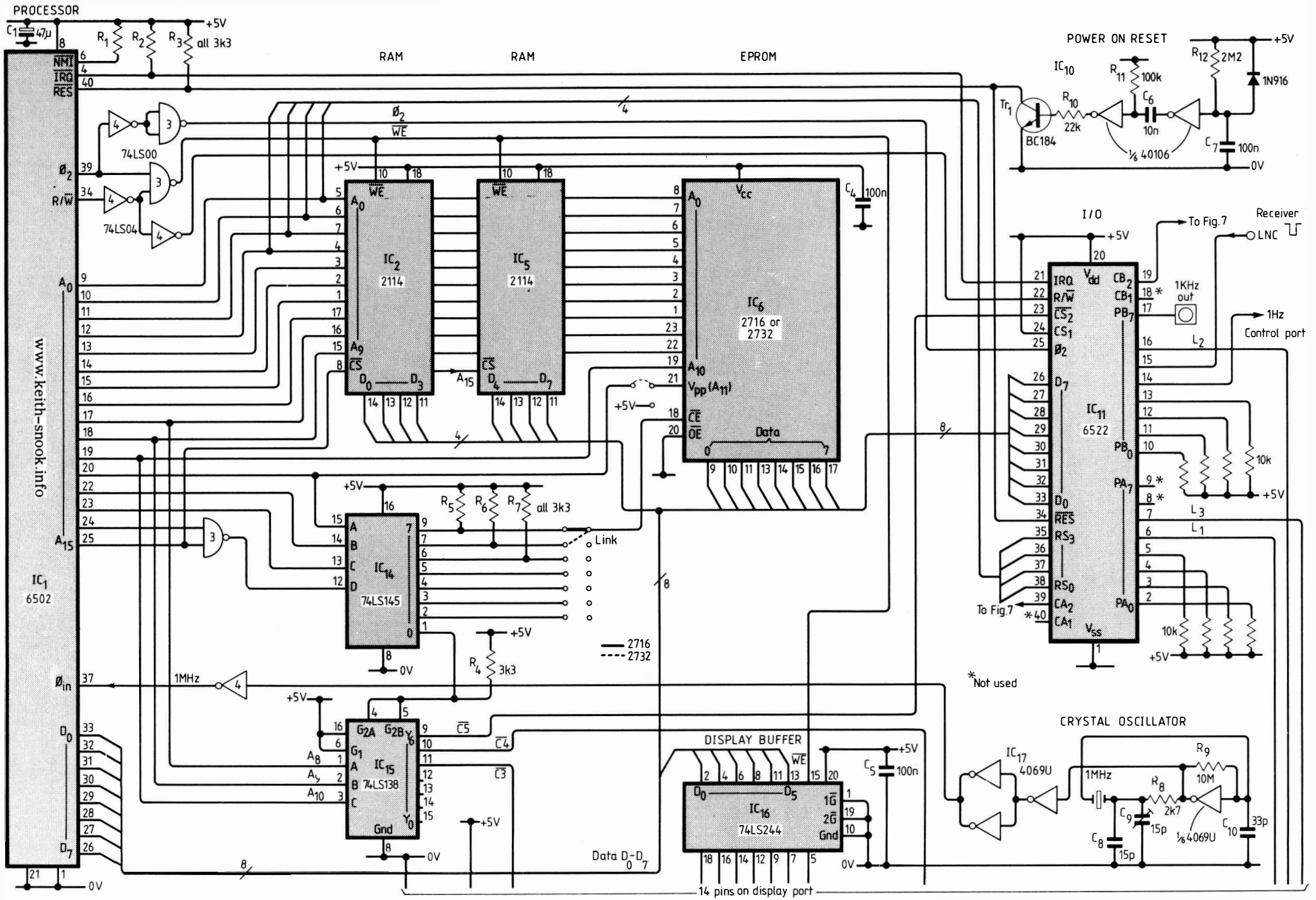


***Fig. 3.** 60kHz slow-code receiver. The tuned transformer is wound on an RM6 pot-core assembly using LA4145 type ferrites. The long-wave receiver coil is wound on an 8 x 5/16in ferrite rod.*



◀ *Fig. 4. Microprocessor decoder*

gating control for the a.g.c. amplifier IC_6. Transistor Tr_3 is a.c. coupled to the undelayed signal and provides a simple time-out arrangement if no modulation is detected. If this occurs Tr_3 remains off permanently and enables the a.g.c. loop. During normal operation, when the carrier is pulsed off for up to 500ms, Tr_3 remains on, the transmission gate opens and switches the a.g.c. integrator to the hold state. This action prevents the gain rising during the normal off periods which would otherwise cause noise to be amplified and excessive overshoot in the received carrier level, which in turn causes timing errors in the demodulated signal.

The d.c. amplifier is followed by a simple active low-pass filter and a Schmitt-trigger level sensing stage which provides a logic level output, high corresponding to no carrier. This output is inverted and buffered for t.t.l. compatibility. Complementary m.o.s. apmplifiers are used throughout to reduce the current requirements and dispense with dual supply rails.

Micro decoder

The complete decoding system is based on a 6502 microprocessor. Although this device is not the most powerful in terms of number crunching, its memory-mapped architecture and addressing modes make it an ideal choice for industrial control appli-

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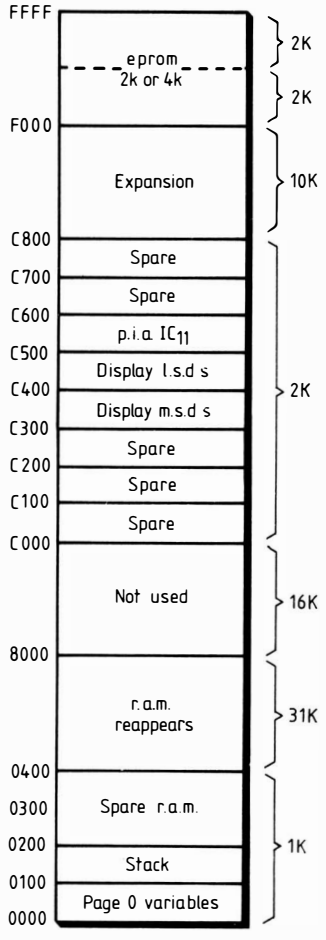

Fig. 5. Memory map.

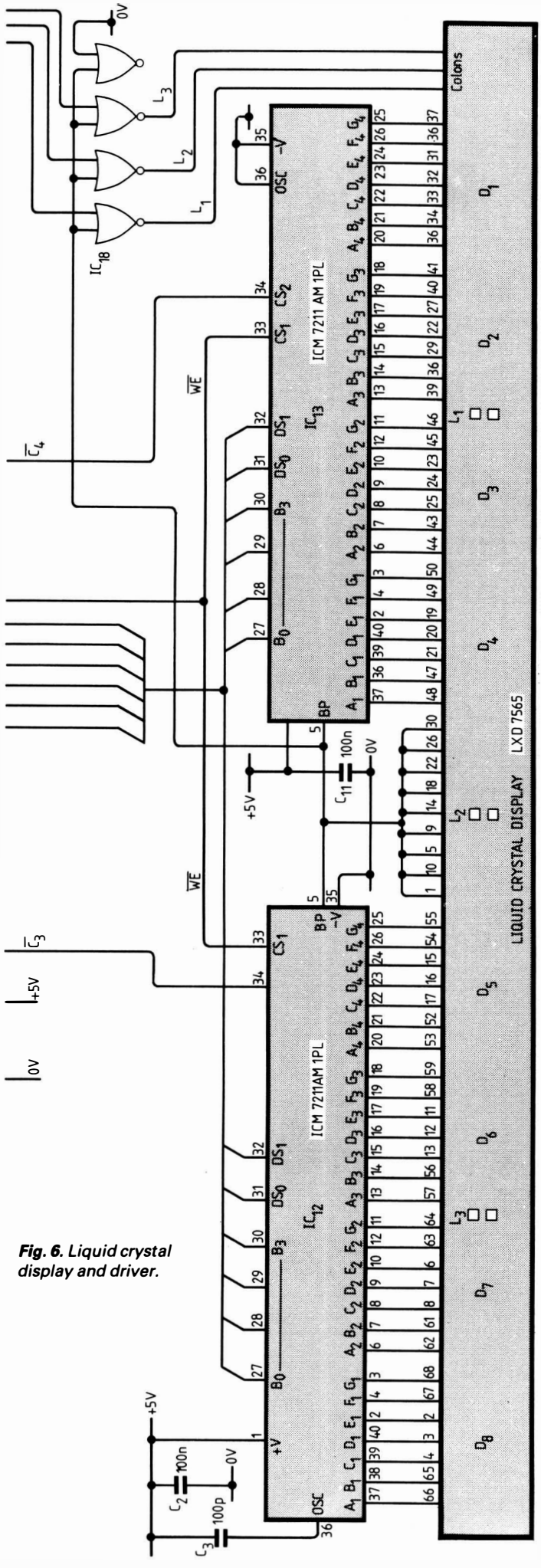

Fig. 6. Liquid crystal display and driver.

conds necessary for conventional input/output procedures. However, because of the automatic address incrementing performed by the d.m.a. controller, new address pointers have to be entered before the selected location exceeds the available memory space. It is convenient to manipulate the audio samples in blocks, and to re-initialise the d.m.a. controller at the end of each block. The execution time of the software routine controlling this function must, of necessity, be shorter than the audio sampling interval, otherwise samples could be lost. This segment of code is therefore designed around register manipulation instructions which are much faster than memory accessing operations. Software for the complete system, capable of rapidly switching between 14-bit linear (uncompanded), 14: 10 A-law and 14: 10 near-instantaneous companding algorithms, occupies less than 1000 words.

Subjective tests of the system described have confirmed that the effect of 14: 10 digital companding, whatever the algorithm, is inaudible with normal programme material, but discernible when pure tones are transmitted. Results from other workers in the field[4] show that 14: 10 near-instantaneous companding provides a standard of performance virtually identical with uncompanded sound. This is likely to be of great importance for satellite transmission, where significant savings in capital plant can be achieved if more channels can be accommodated within a given bandwidth.

Future techniques

Voice synthesis by microcomputer is a rapidly developing technique, especially for electronic toys and games. Most such devices currently available appear to possess American or Japanese accents, so revealing their places of origin. Economy of storage and audio bandwidth is afforded by masculine voices, but this is likely to become a minor consideration as the cost of memory chips continues to decline. Solid-state recording of high-quality musical performances is a more difficult matter, unlikely to be solved by the silicon chip for many years hence. For example, any recording of Beethoven's ninth symphony would require a digital storage array of approximately 2000 megabits. Current prices of memory chips would need to fall by a factor of 100 000 to render viable any such scheme. Meanwhile, more traditional devices such as magnetic tape, hard disc storage and the newer 'Winchester disc' continue to improve in performance, possibly rivalling the storage density achieved by laser-optical techniques.

In the digital processing area, one of the more interesting new devices to emerge is the Intel 2920 processor. This comprises an analogue-to-digital converter, a signal-processing computer and a digital-to-analogue converter, all contained on a single silicon slice. Current technology limitations restrict its operating frequency to about 14 kHz. However, speed improvements to at least five times that figure, whereby it would admirably suit the needs of the digital audio engineer, can now be expected. □

References

1. Sanchey, A A, 'A new ultra-linear 16-bit digital-to-analogue conversion system for professional audio'. 66th AES Convention, Los Angeles, 6-9th May 1980.
2. Jones, A H, 'Digital Coding of Audio Signals for Point-to-Point Transmission'. Publication 166, IBC London 1978.
3. de Lamare E, 'Le Codage numerique des signaux sonores de haute qualite. . .' *Revue de Radiodiffusion-télévision*. No 44 Sept-Oct 1976, pp 12-33.
4 Gilchrist, N H C, 'Digital Sound Signals: Tests to compare the performance of five companding systems for high quality signals'. BBC Research Department Report, RD 1978/26.

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cations. And because the 6502 has been chosen by many of the microcomputer manufacturers, continued production seems assured for the forseeable future.

The hardware shown in Fig. 4 has been kept as standard as possible to reduce the overall cost, and the memory map for this arrangement is shown in Fig. 5. Circuits IC_2 and IC_5 provide 1K of r.a.m. for essential variables, the stack in pages 0 and 1, plus spare areas in pages 2 and 3. The r.a.m. is not fully decoded and appears throughout the bottom half of the 64K address space. An e.p.r.o.m. containing the firmware is assigned to the top 2 or 4K of memory with address decoding provided by IC_{14} for an expanded system. Wire-ORing of the address decoder outputs provides addressing options. Circuit 15 is enabled at C000 (hex.) to provide sub-divided outputs for display drivers and a versatile interface adapter.

The system clock is provided by a 1MHz crystal oscillator using unbuffered c.m.o.s. gates. This also provides the timing for a back-up system and is trimmed for best results in this mode. Power-on reset is provided by two Schmitt inverters which allow the power supply to stabilize before the program is initiated.

A potentially troublesome source of interference for v.l.f receivers is the conventional multiplexed display, and for this reason a low-current liquid crystal type is recommended. A suitable display and driver circuit which will plug directly into the display port is shown in Fig. 6. The eight-digit panel allows six 0.5in digits to be displayed with spaces to improve legibility. The control port of IC_{11} allows different displays to be selected. It is important to use only the AM version of the 7211 display drivers as these include display blanking and a microprocessor interface. Because the display port has been designed to drive remote displays via a short length of ribbon cable, IC_{16} is necessary to buffer the 6502 data bus.

As well as displaying time and date information, the evaluation system can be used with other equipment via an RS232C interface which transmits ASCII information. The necessary hardware additions are shown in Fig. 7. IC_7 divides the 1MHz clock to provide a 2,400 baud generator, and IC_{19} converts the serial data from the v.i.a. to an RS232 level.

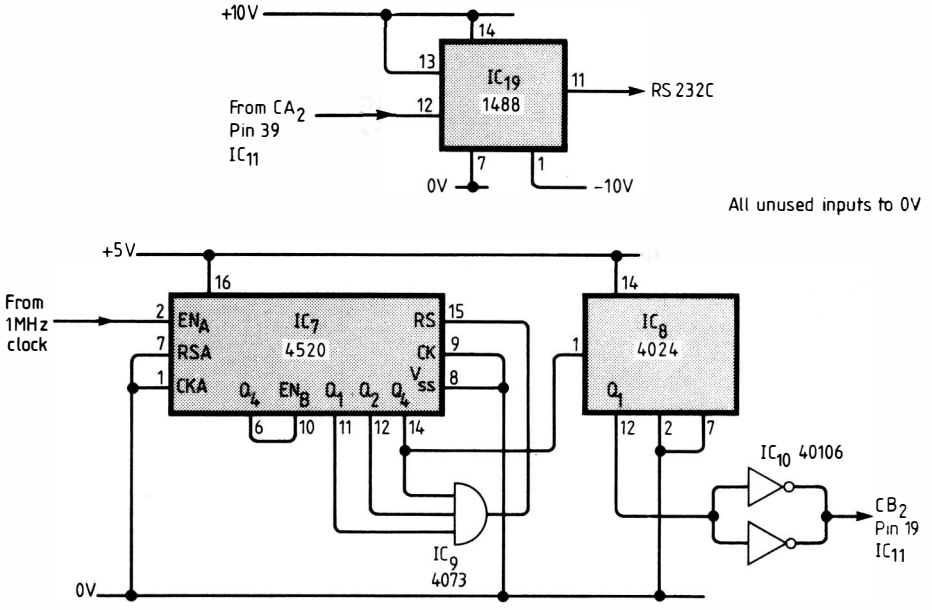

Fig. 7. RS232C generator and level translator.

Part two of this article describes firmware, construction and testing. A complete kit of components for this design will be available from Circuit Services, 6 Elmbridge Drive, Ruislip, Middx (telephone Ruislip 76962).

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Based on a 6502 microprocessor, this clock decodes and displays serial information from a v.l.f. receiver. Although requiring powerful and complex firmware for best possible performance in difficult areas, a system for non-critical applications can use only 2K of object code. This second article describes alignment and firmware for a basic clock which can be contained in a low-cost 2716. For future expansion, this ram can be replaced by link selection with a 2732 device.

by N. E. Sand

Because most of the processing is real-time, fast and efficient assembly language must be used to decode and display the transmitted information. In the flow chart for the basic clock, shown in Fig 1, the program starts with a short initialization sequence which sets the interface adapter i/o configuration, the timer for regular 1ms interrupts, and clears part of the ram area. After initialization, the processer enters the main software loop which is followed continuously. Flags are passed by routine which mainly maintains a series of timers. The receiver output is sampled in the main loop by a routine which searches for level changes from low to high or *vice versa*. When a change is detected, one of the timers is read and reset. The low-to-high transition usually occurs at the end of a carrier break, the duration of which determines a logic 1 or 0 in the serial code.

Invalid timer values signal error conditions which reject the block of code being received. The various double pulses that occur in the code are detected and ignored. While the main program loop is operating, a continual search is made for the unique eight-bit synchronizing sequence 01111110 which indicates the end of each time frame. When this sequence is recognized, a further timer, also updated by the 1ms interrupts, is initialized. On time-out a window is set for a further short period, during which a high-to-low transition in the receiver output will synchronize the decoded seconds counter and relevent timers. A software loop is then initialized and maintained in-phase with the received second pulses.

The display is updated whenever a change could have occurred in the display registers. Digit-select codes are set with the relevant data for each digit, and strobing of the display drivers is achieved by writing to these locations in sequence using the chip selects inputs. When the decoded seconds count and timer are at a certain value the error status, including a parity check, is examined and if error-free, the decoded time is transferred to the back-up clock.

This design provides better error protection than the parity bit alone can offer, and does not use too much memory space. A commercial system which offers foolproof operation requires greatly extended error detection and analysis together with optimization techniques to maintain accuracy; far more memory space would be needed to accommodate the software and this would depart from the "evaluation-system" concept. The present design provides good performance in normal operating conditions and only requires one 2K rom. A high interrupt rate provides good measurement accuracy and resolution in the timers. Overall accuracy of the clock after synchronization with the transmission is approximately 50ms.

The most important part of this clock, or any other design based on a time-coded transmission, is the receiver. Although complex logic circuits or powerful software and microprocessors can be used to detect and analyse any error or noise transient in the transmitted code, unless a carefully designed receiver is used in conjunction with this processing, practically every clock or code will be rejected and the clock will suffer from the usual crystal drift over long periods, or worse still, will not be

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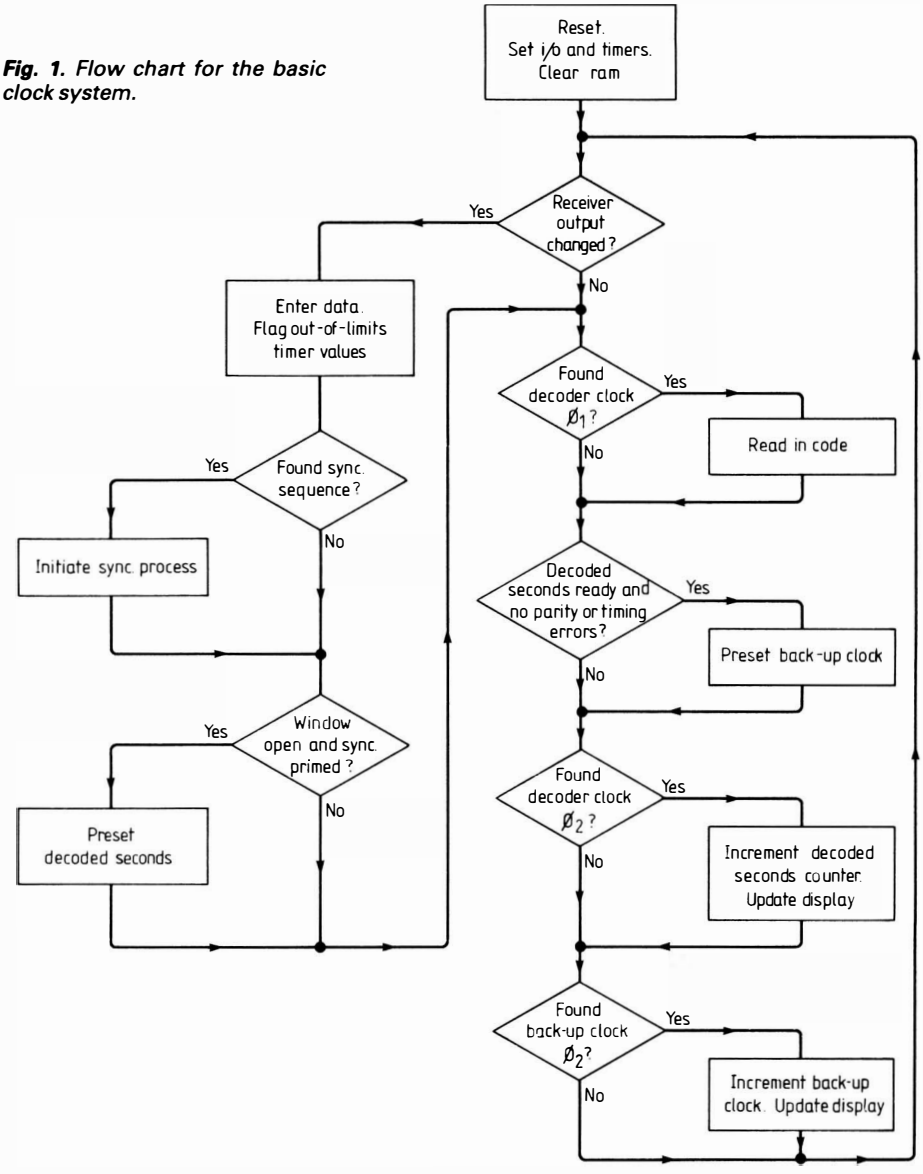
***Fig. 1.** Flow chart for the basic clock system.*



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automatically set after switch-on. This receiver design was chosen as a good compromise between the complex and more costly professional receivers and the simple phase-locked loop or r.f. i.c. designs which, due to the special interference problems, do not operate satisfactorily at v.l.f. without careful positioning of the aerial. Provided that care is taken with construction and alignment, this receiver will provide good performance in most conditions and at long range.

The 3dB bandwidth of the tuned circuit is about 300Hz, so if a signal generator is used it must be set to 60k ± 30Hz. Short the receiver input at the aerial terminals and adjust the potentiometer for 4V at the output of IC_1. Remove the short, set the aerial trimmer capacitor to the mid point, and position the aerial coil so that the centre is about 65mm from the centre of the ferrite rod. Adjust the tuning core of the transformer for maximum output at IC_4, ensuring that a true reading is achieved by tuning well through the maximum and back again. With eccentric adjusters, two or even three smaller peaks can be encountered. Carefully slide the aerial coil along the ferrite rod to maximize the output at IC_4 (usually around 1.35V) and secure the coil with melted wax. Finally, peak the tuning with the trimmer capacitor and recheck the adjustment of the transformer.

When correctly tuned to 60kHz the receiver produces regular inverted pulses at the output. Resistor 9 has been included to disable the a.g.c. loop and is normally left disconnected as shown. When the clock has been assembled and the receiver aligned, feed the receiver output to pin 15 of the v.i.a. and check that a 1Hz output is produced at pin 14. If no output is present, test the receiver output, check that the supply voltage is present on all i.cs and check that the oscillator is operating correctly. Connect the display board and check that the correct time is loaded into the registers. This may take two or three minutes after switch-on, depending on where in the code the processor starts to operate. When the correct time appears, select the date display by switching pin 10 of the v.i.a. to 0V. The remaining pins on the control port have been provided for future expansion to select and control other functions. If sporadic operation occurs check that the aerial is not in the signal-null position (axis pointing to the transmitter) and check for sources of local interference such as television receivers, lamp dimmers and noisy fluorescent tube fittings. □

A kit of parts for the clock is available from Circuit Services, 6 Elmbridge Drive, Ruislip, Middx (telephone 71 76962). Copies of the object code listing are obtainable from the editorial office, in return for a stamped envelope.