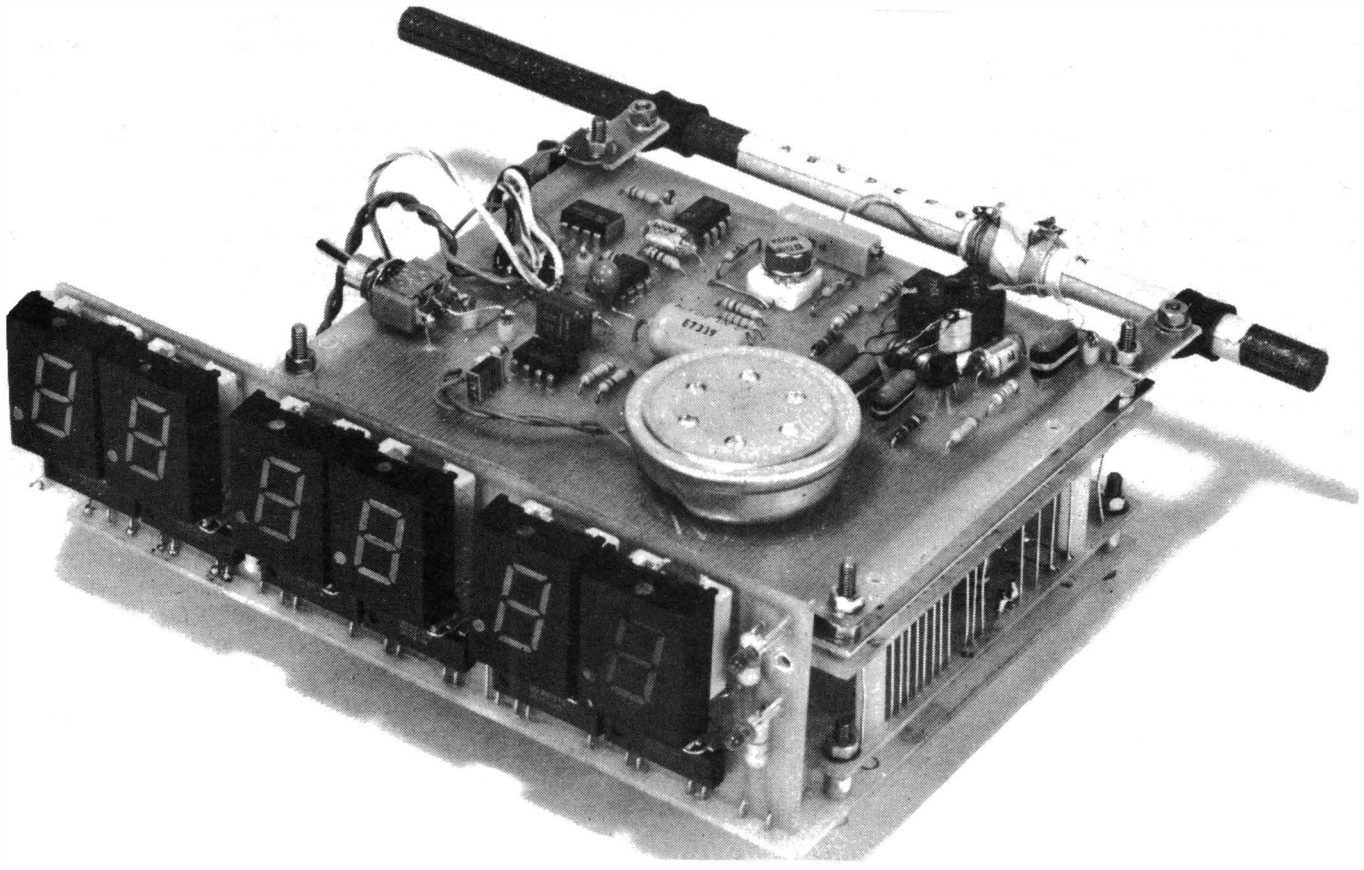
Self-setting time code clock

Constructional design suitable for domestic use

by N. C. Helsby M.A. University of Essex

To meet the demand for a fully constructional time-code clock this article describes a modular design comprising five basic functional units. The full circuit receives a time-coded transmission from Rugby MSF and uses this to drive a six-digit display. An optional GMT/BST converter accounts for the one hour discrepancy which exists during the UK summer.

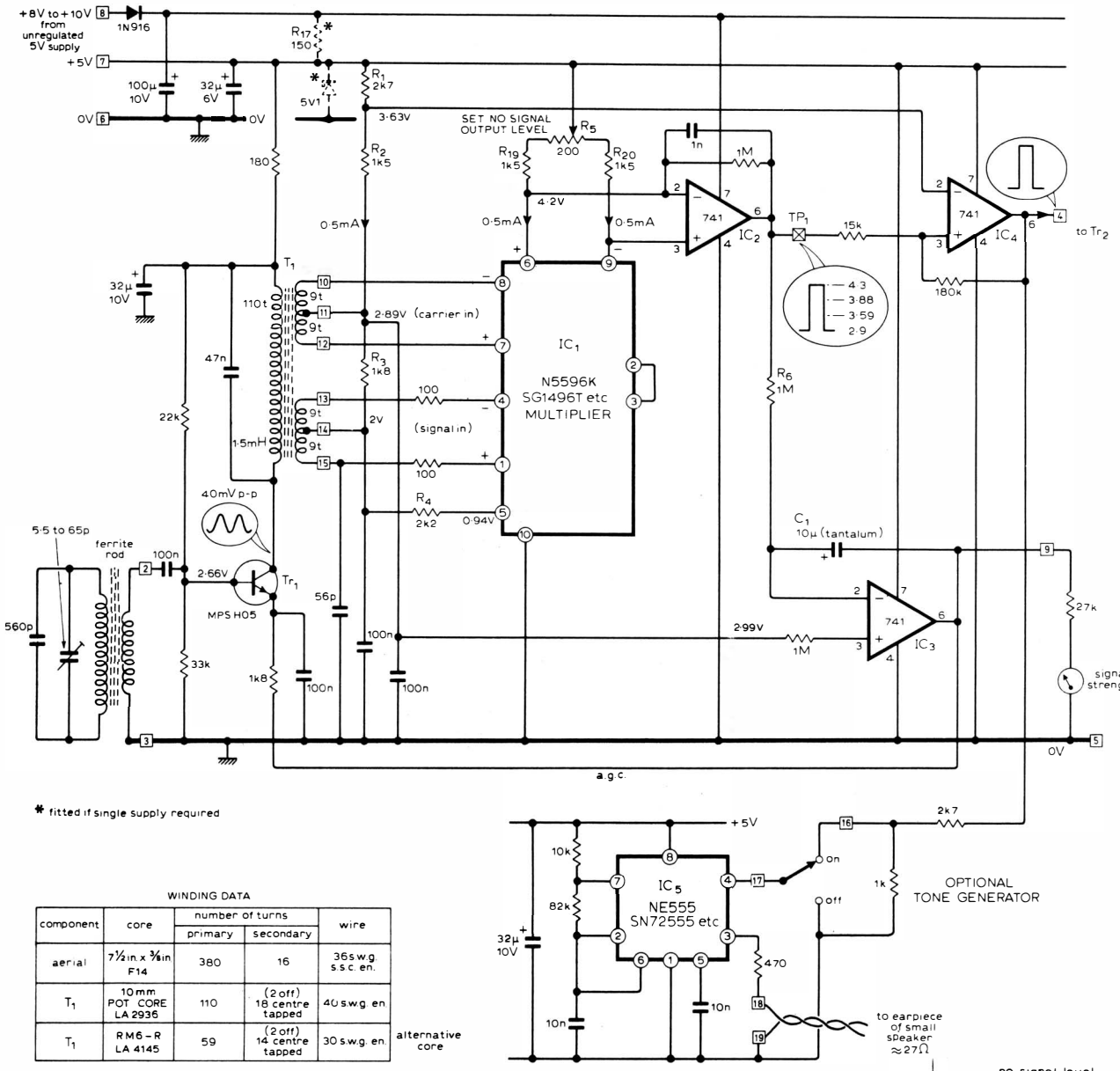


Self-setting digital clocks using coded radio signals have recently been made possible in this country by the introduction of a time-of-day code into the 60kHz transmissions from Rugby, call sign MSF. Until recently only second and minute markers were transmitted in addition to the call sign. This service is maintained as before but the transmission now carries a 13-bit b.c.d. code giving hours and minutes in the UTC time scale.

Receiver

Various receiver designs were considered including a phase-locked loop version. However, it was desired to keep the circuitry simple and a receiver with two tuned stages of amplification followed by a detector was found to work well with a pre-set gain control. With this conventional design it was difficult to obtain more than 12dB extra gain over that required at 100 miles from the transmitter. To obtain extra sensitivity without the danger of regeneration, a low-level detection system was designed using a multiplier as shown in Fig. 1. By operating the multiplier as a frequency doubler a d.c. output is obtained in addition to the double frequency which is removed by filtering. Most of the gain is required at audio frequencies and is provided by amplifier IC_2. Using this system, no high levels of 60kHz are present in the receiver which eliminates pick up by the ferrite rod aerial. Although the signal strength has been found consistent, inclusion of a.g.c. and a precision Schmitt-trigger level detector enables best use to be made of the available signal at any moment. The signal strength meter is a useful addition and allows optimum positioning of the aerial.

The multiplier is preceded by a common-emitter gain stage with a tuned collector load, the input of which is fed by the aerial. Current in this stage is set by the a.g.c. amplifier, and reaches a maximum of about 1mA under no signal conditions. Resistors R_1 to R_4 set the multiplier tail currents, signal and carrier input bias levels via centre tapped windings, the a.g.c. amplifier reference, and a reference for the Schmitt-trigger comparator circuit. Half a milliamp flows in each of the multiplier loads under no signal conditions. Output of IC_2 is set to 4.3V by R_5 when no signal exists (shorted aerial). When a signal is applied to the input of



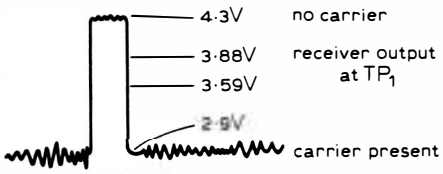
WINDING DATA

component	core	number of turns		wire
		primary	secondary	
aerial	7½in x ⅜in F14	380	16	36 s.w.g. s.s.c. en.
T_1	10mm POT CORE LA 2936	110	(2 off) 18 centre tapped	40 s.w.g. en.
T_1	RM6-R LA 4145	59	(2 off) 14 centre tapped	30 s.w.g. en.

alternative core

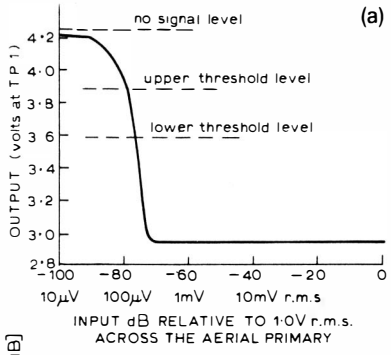
Fig. 1. Receiver using a multiplier as a frequency doubler to produce a d.c. output. Most of the gain is at a.f. which eliminates aerial interference from high levels of 60kHz.

Fig. 2. Typical break in carrier relative to the Schmitt-trigger levels.



the receiver the negative differential output of the multiplier is amplified and filtered by IC_2 (if output is not negative either of T_1 secondary windings may be reversed). The a.g.c. amplifier IC_3 produces a level of 2.9V at the output of IC_2 by controlling the gain of Tr_1. The long time constant formed by R_6 and C_1 ensures that the gain does not change much during the 0.1 to 0.5 second breaks which occur in the carrier. This slow response causes a delay after switch-on for the signal to appear. Schmitt-trigger IC_4 has a 0.29V hysteresis and the thresholds are 3.88 and 3.59V. These levels were chosen because most of the noise appears when the carrier is present. A typical break in the carrier relative to the Schmitt-trigger levels is shown in Fig. 2.

The receiver is required to respond to a 60kHz carrier modulated by pulses, the shortest of which is 5ms. Because single tuned stages are used there is no overshoot in the response and the rise time of a stage is $0.7/B$ where B is the bandwidth in Hz between the 3dB points. This expression accounts for the two sidebands of the modulated wave occupying a frequency band that is twice the modulating frequency. If the response determining stages have similar rise times the exponential output of the receiver $V = V_0(1-e^{-t/\tau})$ where t is the time after a step of carrier is applied, V_0 is the final output after a long period and τ is the response time constant.



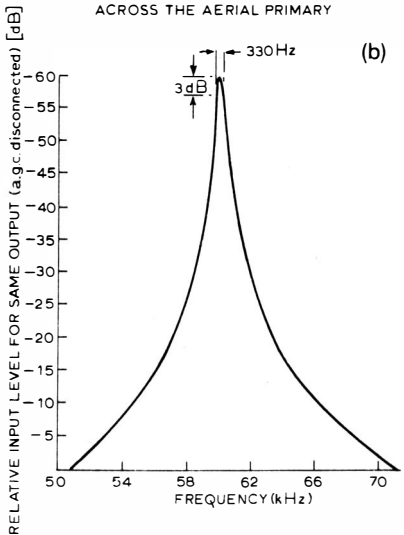


Fig. 3. (a) Minimum input voltage at aerial to produce a low output from IC_4. (b) Frequency response of receiver.

The rise time (T) is the time taken for V in this equation to rise from $0.1V_0$ to $0.9V_0$ and can be expressed as 2.2τ. Therefore, $V = V_0(1-e^{-2.2t/RT})$. From this equation the overall rise time which will allow V to reach 99% of V_0 in a specified time t may be found; $0.99 = 1 - e^{-2.2t/RT}$ therefore $t/RT = 2.0$. Thus if $t = 5$ms the overall time required is 2.5ms. Two tuned circuits in the receiver define RT in addition to the filtering capacitor. The transmitter rise time may also be taken into account in this approximate analysis if it is considered to have the same rise time as one of the receiver stages. The overall rise time is approximately proportional to the square root of the number of stages. For these four response determining stages to give an overall rise time of 2.5ms, each stage should have a rise time of $2.5/\sqrt{4} = 1.25$ms.

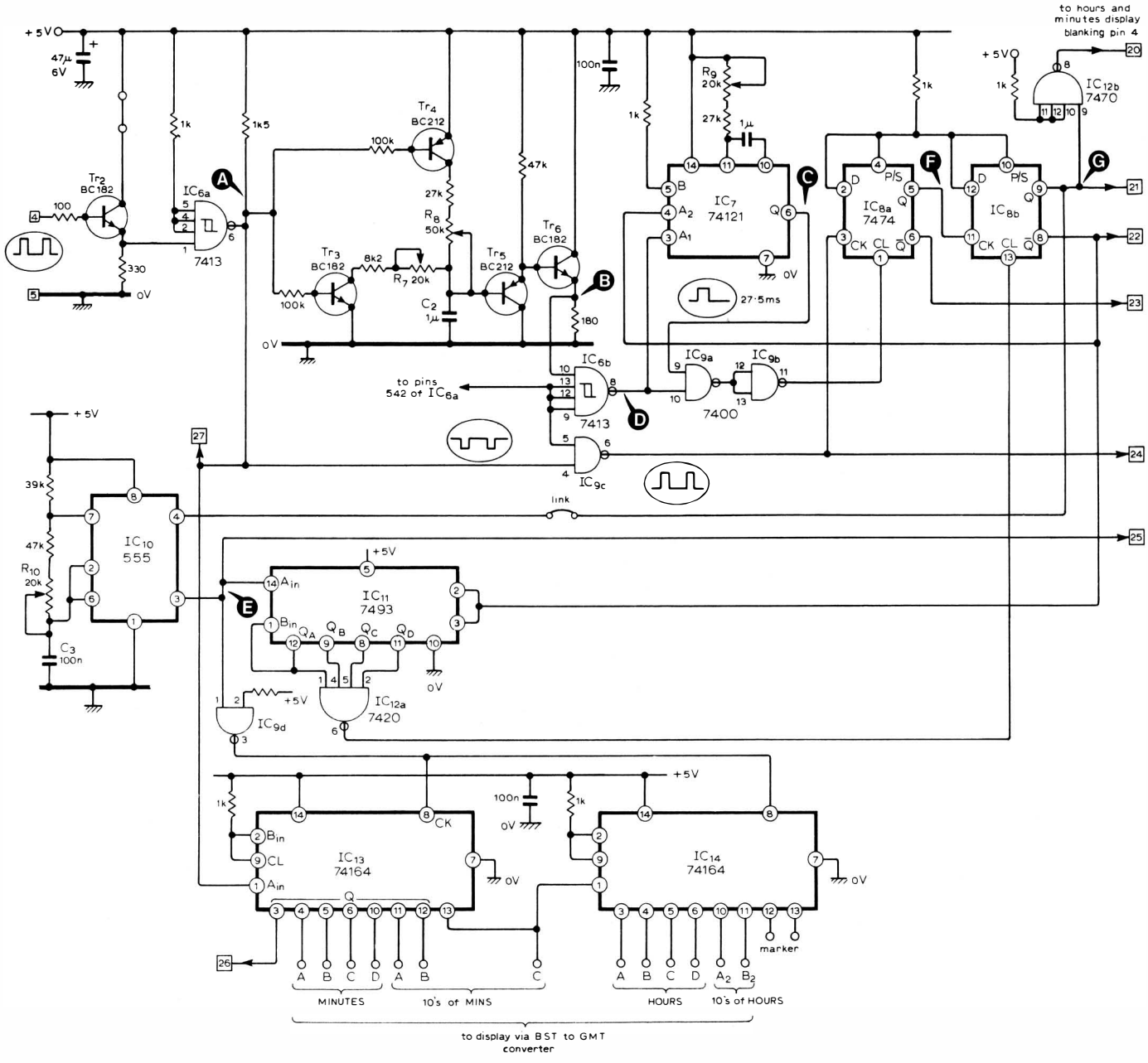
For the single tuned stage, rise time is $0.7/B$ hence B is $0.7/1.25 \times 10^{-3} = 560$Hz. The loaded Q's of the aerial and the amplifier tuned circuits should be adjusted to give a 3dB bandwidth of this order of magnitude, requiring a loaded Q of 110 (60,000/560) at 60kHz. Note that if two single tuned stages have bandwidths of 560Hz the overall bandwidth, which is given by $B = B_0\sqrt{2^{1/2} - 1}$ where B_0 is the bandwidth of each stage, is $0.64 \times 560\text{Hz} = 360\text{Hz}$.

The aerial pick-up coil design involves a compromise between Q and output voltage. Tuning is accomplished by means of a fixed capacitor and a trimmer across the primary coil. It was found that 36 s.w.g. single silk-covered wire gave a Q of about 140 with the coil spread over 2in. A signal generator connected across the aerial primary produced the results shown in Fig. 3(a). The minimum level of signal required to register as a low from the Schmitt trigger is 160μV r.m.s. across the aerial primary. The maximum signal picked up from Rugby, 100 miles from the transmitter, was equivalent to 3.5mV r.m.s. which gave about 26dB reserve gain. Inside a reinforced concrete building the signal was 10dB lower which still left 16dB of gain. Frequency response of the receiver is shown in Fig. 3(b). The a.g.c. was removed and Tr_1 was operated at a current which would normally give the correct output level from a signal of about 1mV r.m.s. across the aerial primary. It should be noted that the step-down ratio of the aerial transformer is 380:16 or 27dB in terms of signal strength. By buffering the input stage, so that this ratio can be reduced or eliminated, greater sensitivity can be obtained.

Decoder

The receiver output detector, which appears typically as an inverted form of waveform A in Fig. 5, is fed into the buffer stage Tr_2 in Fig. 4. This is

Fig. 4. Decoder circuit, the charge and discharge action of C_2 provides heavy filtering and increases the noise immunity.



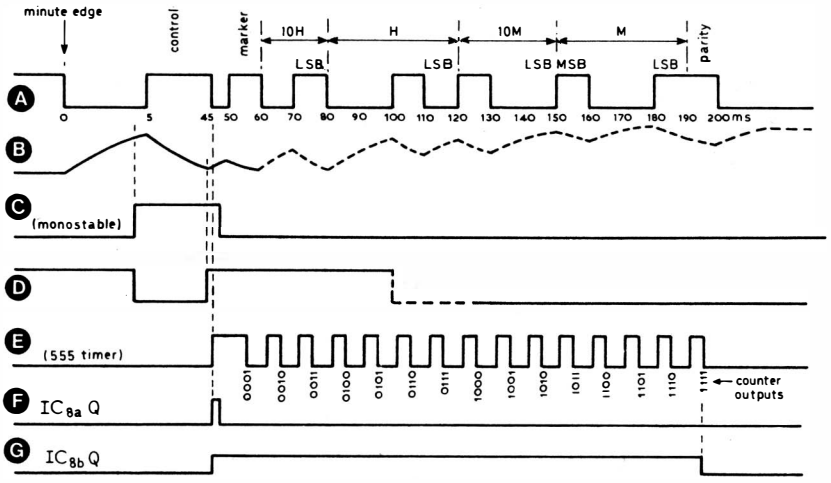
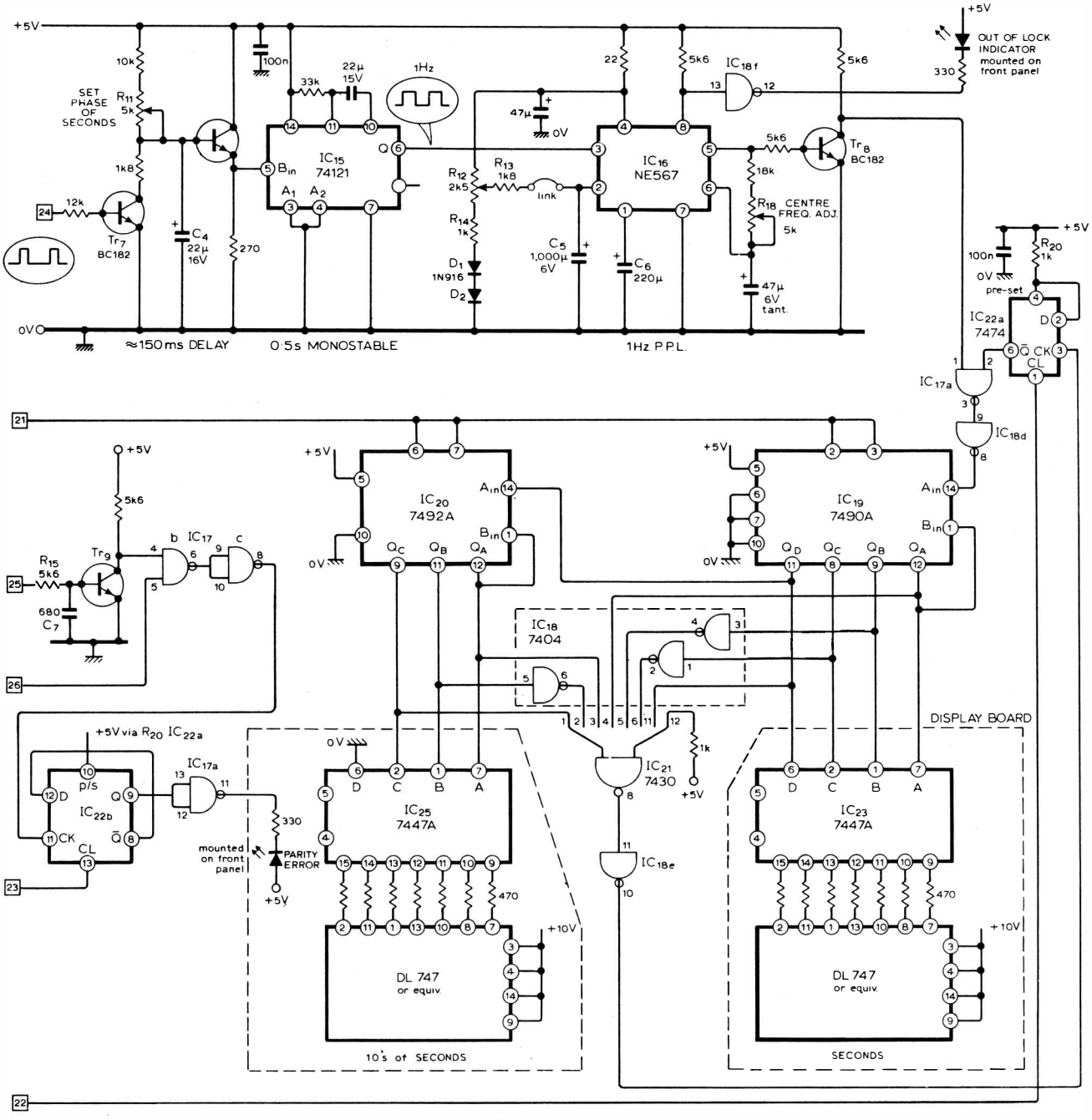


Fig. 5. Waveforms for various points throughout the decoder circuit.

followed by Schmitt trigger IC_{6a} to improve noise rejection in the conversion to t.t.l. levels. The output of this gate feeds a circuit which charges and discharges capacitor C_2 to produce waveform B in Fig. 5. Transistors Tr_5 and Tr_6 form a double emitter follower to drive Schmitt trigger IC_{6b}.

Resistor R_8 is adjusted so that if point A is low for more than 22ms, the positive threshold on the second Schmitt trigger is reached, to produce a low as shown by waveform D, Fig. 5. The output from IC_{6b} triggers monostable IC_7 which is adjusted by R_9 to give a pulse length of 27ms. Output D is required to be high with output C in order to clear IC_{8a} via IC_9. These conditions leave a narrow window during which a negative going edge at A, made positive-going by IC_{9c}, can clock IC_{8a}. Resistor R_7 is adjusted so that if A is high for more than 18ms after the initial 25ms break, C_2 is discharged to the negative threshold of IC_{6b}. The charge and discharge action of C_2 provides heavy filtering and reduces the likelihood of false triggering by noise pulses.

Fig. 6. Seconds counter using a phase-locked-loop tone decoder.



Unused inputs of gates which are required to be high are taken to + 5V via 1kΩ resistors as a precaution against transient noise on the power supply. The Q output of IC_{8a} clocks IC_{8b} which in turn allows IC_{10} to run in the astable mode with a frequency set to 100Hz by means of R_{10}. Simultaneously, the $\overline{Q}$ output of IC_{8b} allows IC_{11} to count the negative-going edges from the timer. On the 15th edge all outputs of IC_{11} go high to give a low out from IC_{12a} which clears IC_{8b}. The last-mentioned then resets and holds the timer. The $\overline{Q}$ output of IC_{8b} returning high also resets IC_{11}.

The timer capacitor C_3 normally charges to 2/3 of the supply and discharges to 1/3 by the internal action of the circuit. This gives the mark-space ratio as shown in Fig. 5 with the component values selected. When held in the reset state, C_3 becomes discharged and it is therefore required to initially charge from zero to 2/3 of the supply which produces the first wide pulse as shown. Thus, by choice of resistor values it is possible to place the negative-going edges of the timer output in the centre of the time code bits. This output is then inverted so that the time code is clocked serially into shift registers IC_{13} and $_{14}$ at the middle of each bit; the shift registers clocking on positive-going edges. The registers are not cleared in this design, new information simply pushes out the previous pattern. Although the marker bit can be used as the first received high at the end of the shift registers, to stop the clock, the counter was used because if the marker bit were missed due to noise, the time-code might still be retained correctly.

It is possible that the time code itself contains a pattern similar to the one that indicates the start of the code because it is divided into 10ms-long bits. However, the $\overline{Q}$ output of IC_{8b} is connected to the A_2 input of IC_7 and this pin therefore goes low just before the end of the monostable pulse. IC_7 cannot fire again until the complete code has been received and when this occurs A_2 returns high without firing the monostable so good noise immunity of the code recognition circuitry is maintained.

Seconds counter

Due to the tranmission accuracy, reception and display of seconds is well justified. In this design the Signetics NE567 p.l.l. tone decoder has been used for the seconds counting function as shown in Fig. 6. The device operates from a 5V supply and incorporates a balanced multiplier type of phase detector which, when overdriven, also operates as exclusive-OR gating.

The maximum recommended timing resistance for the p.l.l. current-controlled oscillator (c.c.o.) is 20kΩ. The tantalum timing capacitor may increase in value by as much as 5% for a 20degC rise in temperature but, as the oscillator is not required to accurately run for long periods without an input signal, the effect is not important provided the loop remains locked.

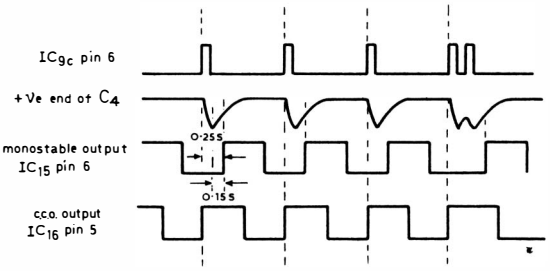
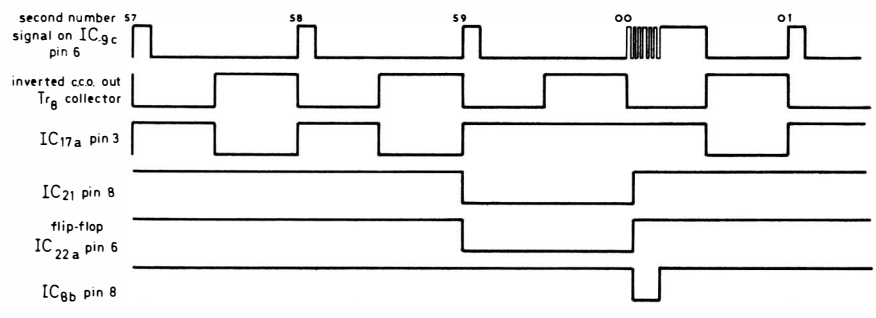


Fig. 7. Delay of 250ms is created from the positive edge on IC_{9c} by lengthening pulses via monostable IC_{15}.

In this application the p.l.l. is required to lock to a single fixed frequency so it is desirable that the bandwidth of the loop is small. Because heavy filtering is used it is necessary to reduce the loop gain which increases damping. This is accomplished by the manufacturer's recommended method of adding $R_{12,13,14}$, $D_{1,2}$. This network reduces one of the internal multiplier collector loads and hence the loop gain. Potentiometer R_{12} enables the correct d.c. conditions to be maintained while the diodes provide temperature compensation. The detection band is reduced from ±7% to about ±4%. Reduction in gain coupled with the value of C_5 gives the loop a damped response which prevents overshoot in phase after a disturbance. It also has the advantage of reducing the number of input cycles required before locking occurs, usually less than the maximum of twenty.

To produce the required 1:1 mark-space ratio at the input of the p.l.l., monostable IC_{15} is used to lengthen the input pulses. By delaying the input to the monostable a phase shift brings the c.c.o. output in phase with the second markers. The total delay is 250ms from the positive-going edge, on the second, at pin 6 of IC_{9c} – see Fig. 7. By timing the delay from the negative-going edge the extra amount required is 150ms which is obtained by allowing C_4 to charge through R_{11}. This capacitor is discharged by Tr_7 when the output from IC_{9c} is high for 100ms after the second. The monostable Schmitt trigger input is used and R_{11} adjusted until the necessary delay is achieved. The output-pulse length of the monostable is fixed at about 0.5s and any phase error can be eliminated by adjusting R_{11}.

Fig. 8. Waveforms present in the seconds counter.



The c.c.o. output is fed via buffer stage Tr_8 through IC_{17a} and IC_{18d} to the input of the seconds counter. The outputs of the counters IC_{19} and IC_{20} are inverted where necessary to present all highs to IC_{21} at the count of 59 seconds. This causes the output to go low and clock flip-flop IC_{22a} causing its $\overline{Q}$ output to go low. Further clock pulses via IC_{17a} are inhibited until the flip-flop is cleared by detection of the minute sequence. Thus, if the hours and minutes are not updated the seconds count ceases. When the sequence is correctly received the counters are reset and IC_{22a} is cleared by the output of IC_{8b}. Waveforms of this are shown in Fig. 8.

It should be noted that extra decoupling of the supply to the tone decoder is used. This is to prevent the decoder running as a locked oscillator, with no signal at pin 3, due to small 1Hz spikes on the supply rail from other parts of the circuit. www.keith-snook.info

(To be continued)

Printed circuit boards

Wireless World has arranged a supply of glass fibre boards for the time code clock. The p.c.bs are available as a set which comprises three double-sided and two single-sided boards for the receiver, GMT/BST converters, decoder, seconds counter, and display. The boards mount on top of each other (see photo) to form a compact module which can be housed in a case approximately 8 × 5 × 3in. The set of boards is priced at £13.50 inclusive or £11.00 undrilled.

A set of special components is also available which comprises an aerial assembly, receiver coil assembly (LA4145) N5596K multiplier, MPS H05 transistor, two 1.5kΩ metal-film resistors, and the NE567 tone decoder. This set is priced at £7.50 inclusive. Available from M. R. Sagin at 11 Villiers Road, London NW2.

Self-setting time code clock

2 — Construction

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The time code arrives in serial form which facilitates the process of parity checking. The first shift register output QA in Fig. 4 represents the signal as received by the decoder whilst the 555 timer is running. This clock signal is taken to the input of IC_{17b} in Fig. 6. The clock itself is delayed a few micro-seconds by R_{15}, C_7 and Tr_9. The delayed clock is taken to the other input of IC_{17b}. Therefore, if QA is high the delayed clock pulse causes IC_{17b} output to go low and clock IC_{22b} via the inverter. If, however, QA is low no clock pulse is received by IC_{22b} and the $\overline{Q}$ output is returned to the D input so that IC_{22b} changes state for every positive clock edge received. The flip-flop is cleared just before the first negative-going edge (waveform E, Fig. 5) when IC_{8a} $\overline{Q}$ is low. Therefore, IC_{22b} commences with its $\overline{Q}$ output high and changes state for every high present in the received signal including the marker and parity bit. Because the marker bit is included in

This second article describes the remaining circuitry and details the construction and alignment procedure using the specified printed circuit boards.

the parity check on reception, IC_{22b} should always receive an even number of clock pulses which leave it with its $\overline{Q}$ output low if parity is achieved. If one of the transmitted bits is incorrectly received the Q output ends high causing an l.e.d. to turn on. Alternatively, incorrect parity could be arranged to blank the display. The output of the flip-flop has been buffered by a spare NAND gate to reduce the effects of wiring to the front panel. This indicator compliments the out-of-lock indicator also on the front panel.

GMT to BST converter

Because the transmitted time code corresponds to GMT, one hour must be added when British summer time is in force. A static code converter (requires no clock pulses) which can be switched in or out is shown in Fig. 9. The six input lines of the hours and tens-of-hours display decoders are fed, without the converter, from the shift register outputs. These outputs have been lettered A, B, C, D, A2, B2 and connect to the converter circuitry which is made up of IC_{23}, IC_{24}, IC_{25}, IC_{26} and IC_{27}. They also connect to the data selectors IC_{28} and IC_{29}. When the switch is in the GMT position the data selectors route the shift register outputs to the display decoders as before. In the BST position the outputs of the converter circuitry, lettered A′, B′ . . . are selected and fed to the display decoders. The data selectors function as a six pole two way switch and provide an additional facility. The circuitry for addition of 1 to the hours uses the standard half-adder configuration as shown in Fig. 10. This works for the four bits A, B, C and D comprising the hours up to 9 (1001). At this point the output code becomes 10 in binary (1010) but is required to be 0 (0000) for b.c.d. with a 1 carried to the tens of hours. Thus B′ and D′ are both high when lows are required. With IC_{24c} added the output goes high when the input code is 9 and provides a carry for the tens of hours. It is also fed to IC_{25a} and $_b$ which cause lows on B′ and D′ respectively. The same circuitry is effective at 19 and the only remaining difficulty is 23 hours GMT which is required to be 00 BST. This is achieved

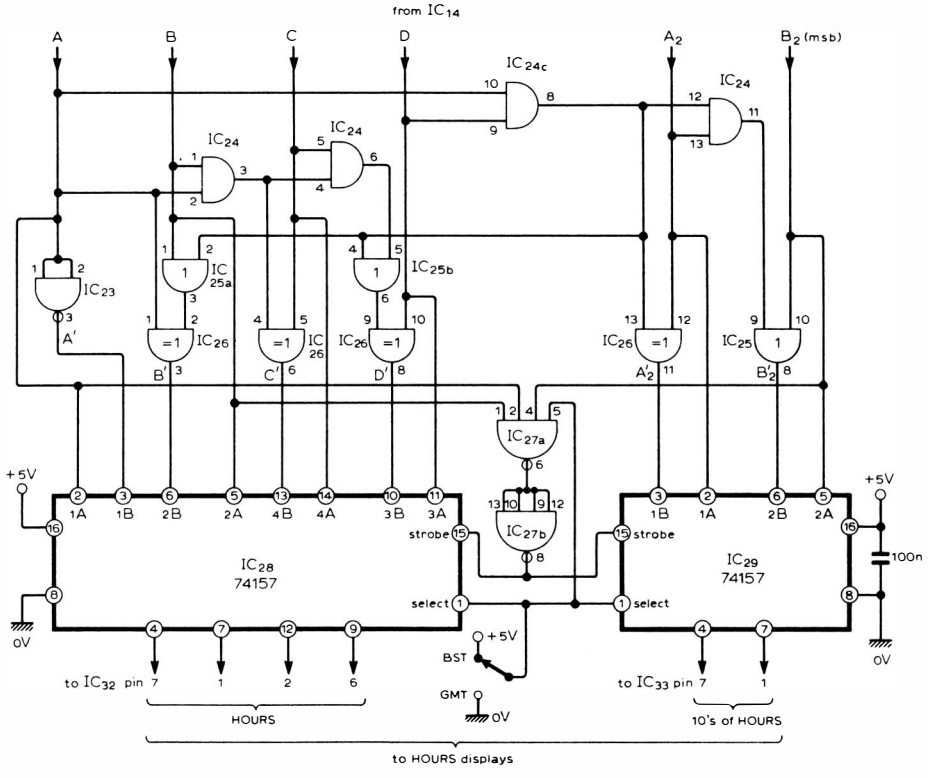


Fig. 9. GMT to BST converter.

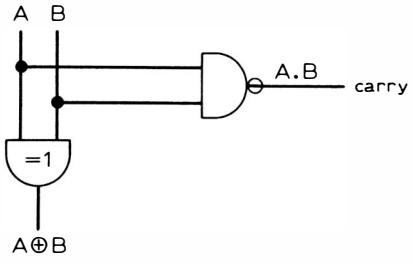


Fig. 10. Conventional half-adder configuration.

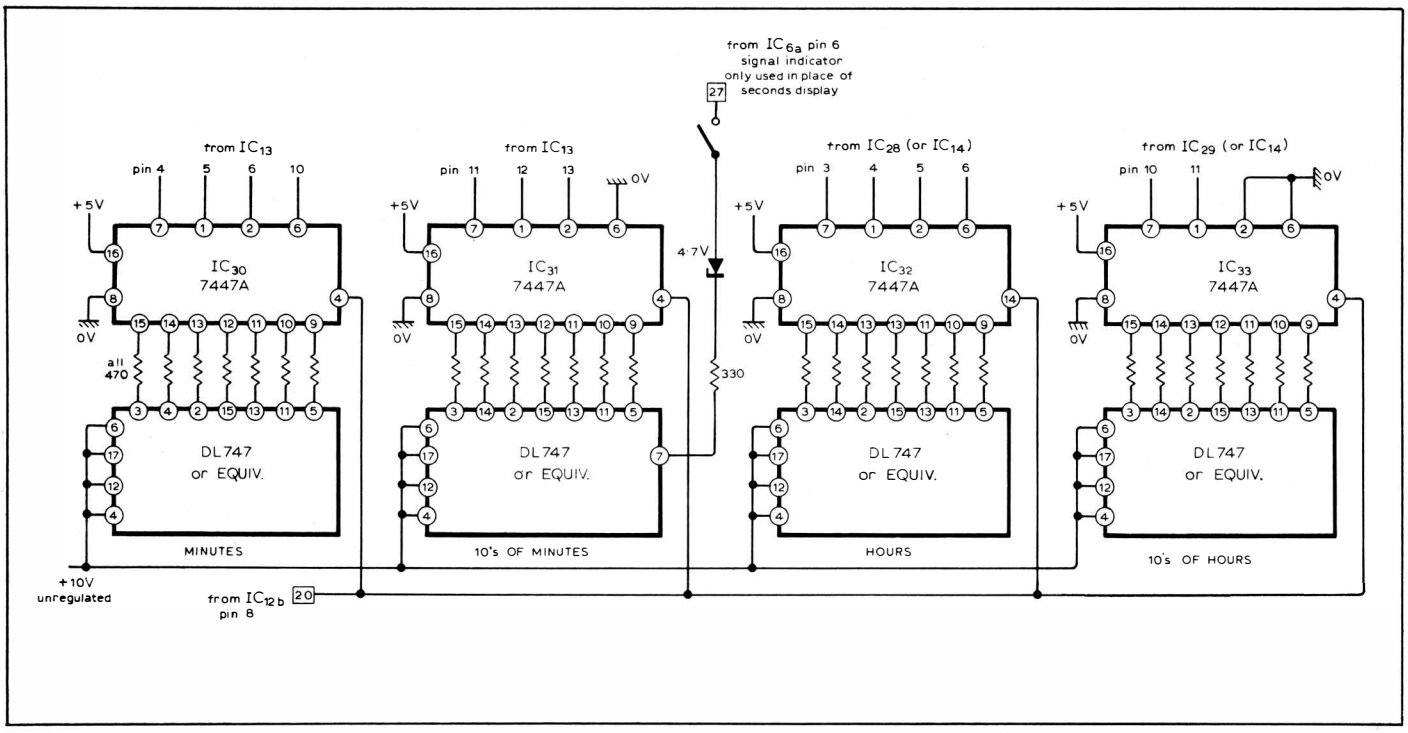
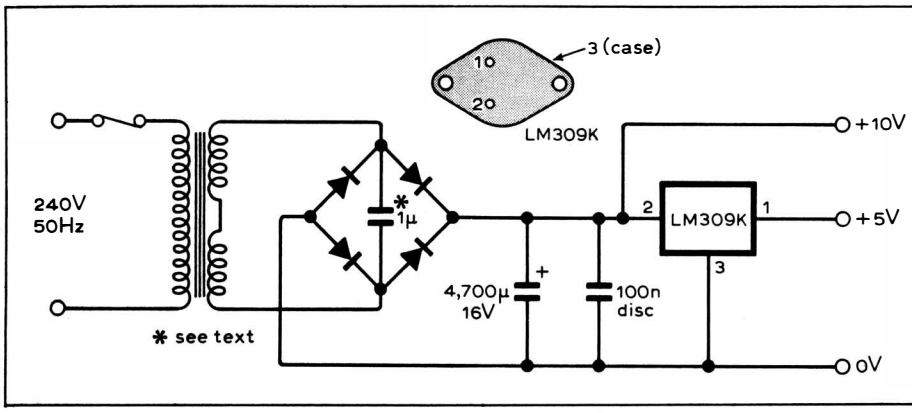


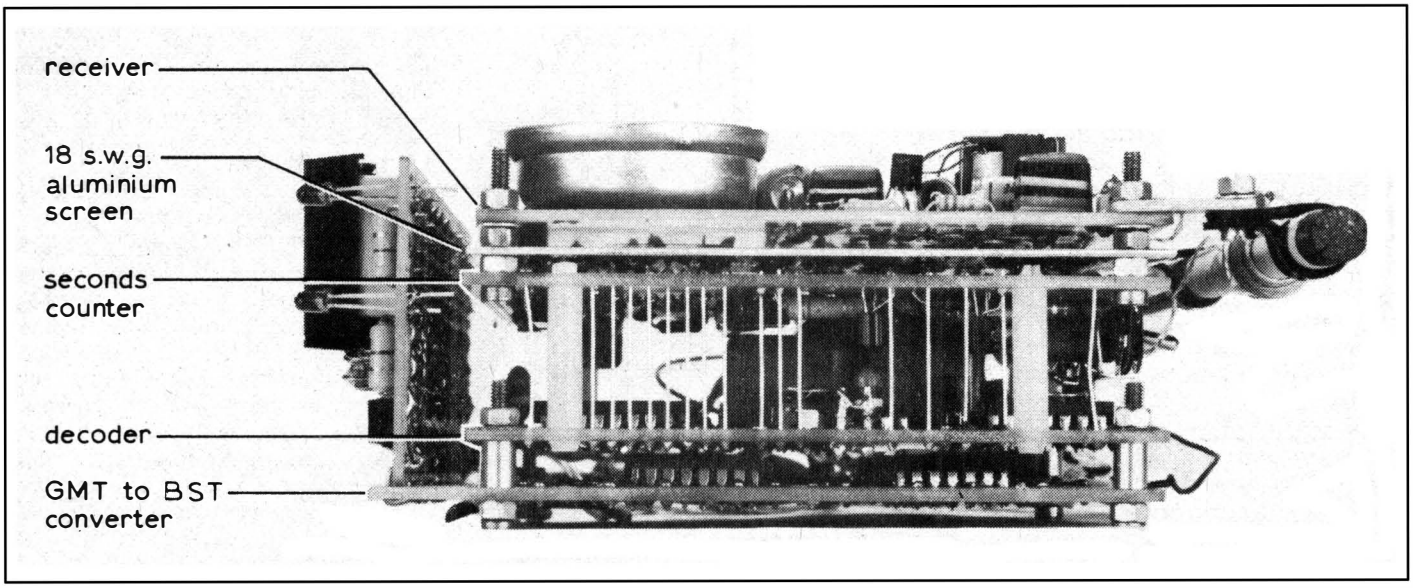
Fig. 11. Hours and minute display. If a seconds display is not used the pulses can drive a decimal point as shown. The 4.7V zener blocks 5V which is always present because the displays are powered from 10V.



Power supply

A single regulated supply is used throughout. The unregulated side of the supply is used to feed 10V to the receiver, and also to the display anodes. A 9V r.m.s. supply is required which may be obtained from a 20VA transformer, 0-4.5V, 0-4.5V, A 1µF capacitor is wired across the secondary to reduce noise radiated from the transformer, due to the action of the bridge rectifier, which may be picked up by the ferrite rod aerial.

Fig. 13. Side view of board assembly. An aluminium screen separates the receiver and seconds counter. The last mentioned and the remaining three boards are all connected via links along edges of the boards. These form hinges so the assembly can be opened out for access.



by detecting 23 when BST is selected by means of IC_{27a} which, via IC_{27b} operates the strobe lines of IC_{28} and IC_{29}. This causes the selector outputs to go low irrespective of their other input states.

The GMT/BST circuitry is applicable to conventional digital clocks in which the time is available in b.c.d. form.

Construction

Five printed circuit board assemblies plus a simple power supply make up the complete design. Connections between these boards are by links which simplify the wiring and assembly, but still allow access to the components by forming hinges along the edges of the boards. The bottom board is the GMT to BST converter onto which is mounted the display board by a row of 26 links as shown in Fig. 13. The decoder board is connected to the converter via 25 links along its front edge. Access to the decoder pre-set controls is through four holes in the converter board. Above the decoder is the seconds' counter board which is connected to the decoder with 17 links along the right hand edge. The seconds' counter board is mounted component-side down, and opens out with the component side uppermost when access is required. Pre-set controls on this board are mounted vertically along its rear edge. The receiver board mounts on top of the seconds' counter, with a metal screen between the two, and its output is connected to the decoder by conventional wiring. The complete assembly of five boards can be mounted in a simple metal case with a power supply and external ferrite rod aerial as shown in Fig. 14. The seconds counter and the GMT to BST converter boards may initially be omitted and added as required; in this case the display board must be wired to the outputs on the decoder.

The receiver uses a single-sided board and wiring is provided to allow single-supply operation. If this is not required the zener diode and R_{17} are omitted and the existing five-volt logic supply is used instead. Resistors R_{19} and R_{20} must have low or well-matched temperature coefficients. Metal film types with coefficients of 50 p.p.m./deg C or better are preferred. Metal oxide types are not suitable unless they have matched temperature coefficients. Two alternative cores are suggested for T_1. The 10mm core is smaller but more difficult to wind and gives a lower unloaded Q Thus, the RM6 core is recommended and winding details are given using this type. The turns ratio has been adjusted to give the same loaded Q value as the 10mm core. The ferrite rod is a 7.5in by ⅜in diameter Neosid F14 type. A former of thin card is made and scramble wound with 380 turns, over 2in length, to form the primary. Over the top of this is wound 16 turns for the secondary. The ends of the primary are connected to the trimmer capacitor which is mounted on one of the aerial support

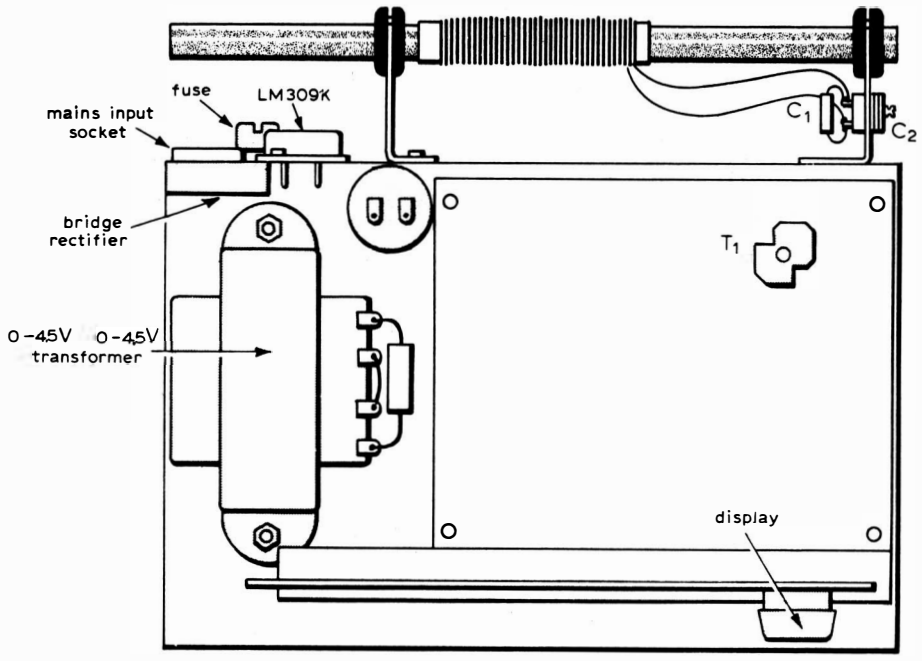


Fig. 14. Recommended layout for clock and power supply.

brackets. Across this trimmer is connected the main tuning capacitor. The ends of the secondary winding are twisted together and taken to the receiver input. Because of the difficulty in obtaining special types of wire the possibility of using a ferrite rod complete with a long wave coil was investigated. A drawback of this scheme is that the inductance of the coil is lower so a higher value of tuning capacitor is required, which means that a suitable trimmer capacitor cannot be obtained. It was found however, that by sliding the coil along the rod, satisfactory tuning could be accomplished. Fig. 15 shows the resonant frequency of the

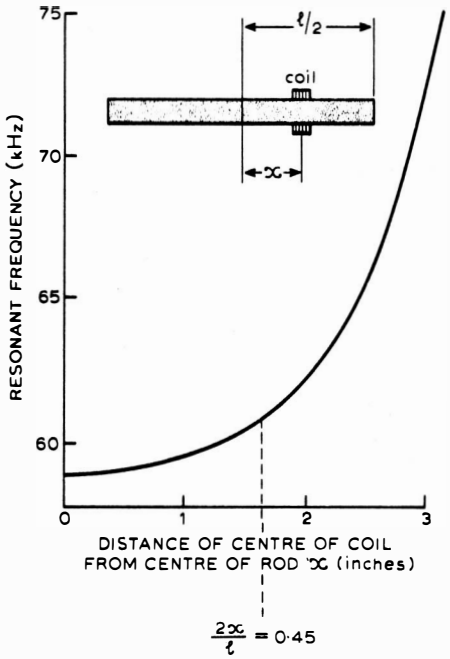


Fig. 15. Tuning aerial by sliding the coil along the ferrite rod.

aerial plotted against coil position. The design position for the coil is 1.7in from the centre of the rod, corresponding to $2X/l = 0.45$ which allows about ±12% adjustment of resonant frequency to cater for variations in permeability. The above measurements were made on the Denco FRAI aerial which has a ½in-wide coil of 180 turns fitted on a 5/16in diameter by 7¾in long F14-grade ferrite rod, shortened to 7½in. A tuning capacitance of 2,500pF is required which gives an unloaded Q of 140 at 60kHz. The wire from the discarded medium-wave coil was used to wind the secondary. Optimum matching into a 1kΩ requires a 12-turn secondary but higher signal levels at both low and high receiver gains were measured with 16 turns. Small polystyrene tuning capacitors are most suitable as they may be fixed to the coil itself leaving only the secondary winding to be connected to the receiver as a twisted pair.

The decoder board is double-sided and wire links must be soldered in position to make connection between tracks on the top and bottom of the board. Note that no links are made via the legs of integrated circuits. Before fitting the four skeleton pre-set poteniometers, holes should be drilled in the board so that these controls may be adjusted from the underside.

To reduce the number of interconnections the display board incorporates the b.c.d. to seven-segment decoders and segment drive resistors, the last mentioned being mounted vertically. The 0.6in displays should be mounted in sockets which can be constructed from 14 pin d.i.l. sockets cut in half. Current for the display comes from the unregulated side of the power supply. This transfers power dissipation to the segment drive resistors. The display board also carries two l.e.ds which give indication of a parity error and loss of lock in the seconds' counter.

The seconds counting board is double-sided and links are made between top and bottom tracks as for the decoder board. The pre-set controls are mounted vertically along the rear edge and may be adjusted from the back of the completed clock. This board links directly to the decoder board by vertical wire links along one edge. The board is first mounted in position, component side down, on four pillars attached to the decoder board. The links are then made and soldered in position. If subsequent access is required the board may be hinged on the links.

Construction of the double-sided GMT to BST converter board is straightforward. Before commencing construction, holes for access to the pre-set potentiometers on the decoder board should be drilled.

Don't forget . . .

● On the p.c.bs several links through the boards have to be soldered both sides. www.keith-snook.info

● Plastics supporting pillars should be used between boards rather than metal types which may cause shorts.

● In Fig. 6 the 47μF tantalum capacitor should be a 10% type. If R_{18} cannot be adjusted satisfactorily the 18kΩ resistor in series can be altered to suit the capacitor.

● Limitation in clock sensitivity is due to the pick up of self-generated interference. For operation in difficult areas screening, or better still a remote aerial, will improve sensitivity.

(To be continued)

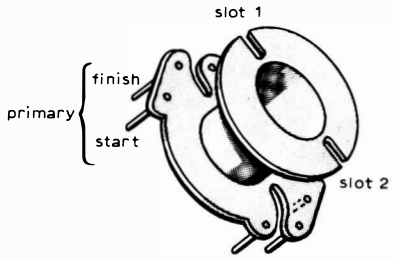
Printed circuit boards

Wireless World has arranged a supply of glass fibre boards for the time code clock. The p.c.bs are available as a set which comprises three double-sided and two single-sided boards for the receiver, GMT/BST converter, decoder, seconds counter, and display. The boards mount on top of each other (see photo) to form a compact module which can be housed in a case approximately 8 × 5 × 3in. The set of boards is priced at £13.50 inclusive or £11.00 undrilled.

A set of special components is also available which comprises an aerial assembly, receiver coil assembly (LA4145), N5596K multiplier, MPS H05 transistor, two 1.5kΩ metal-film resistors and the NE567 tone decoder. This set is priced at £7.50 inclusive.

Available from M. R. Sagin at 11 Villiers Road, London NW2.

Winding details for T_1



Strip enamel insulation from the wire end and carefully solder to the pin marked start primary. Wind 59 turns clockwise (with pins pointing away) and attach to the finish primary pin. Cover winding with ¼in wide tape. Starting with wire in slot 1 leave about 1½in of flying lead, identified as start and wind on 7 turns also clockwise. Form a loop about 1½in. long, twist the loop together and leave this as a flying lead (centre tap) also in slot 1. Continue to wind a further 7 turns exactly, and take the remaining end across to slot 1. Wind a turn of ¼in tape. Repeat the procedure as shown using slot 2. The bobbin now has six flying leads which are in two groups of three, each of which has a start, centre tape and finish. Wire these to the printed circuit board as indicated on the circuit.

Component summary

Resistors — all ¼W, 5%	Quantity
22	1
100	3
180	2
270	1
330	3
470	43
1k	10
1.5k	1
1.5k 2%, matched temp coeff	2
1.8k	3
2.2k	1
2.7k	1
4.7k	1
5.6k	3
6.8k	1
8.2k	1
10k	1
12k	1
15k	2
18k	1
22k	1
27k	2
33k	3
39k	2
47k	1
100k	2
180k	1
1M	3

Preset potentiometers	
500Ω 10-turn cermet	1
2.5k	1
5k	2
20k	3
50k	1

Capacitors			
Types E are electrolytic, T tantalum and P polystyrene			
56pf	P63V	±10%	1
560pf	P63V	±2½%	1
680pf	P63V	±10%	1
1000pf	P63V	±10%	1
4700pf	P63V	±2½%	1
0.1μf	P100V		10
1μf	E100V		3
10μf	T6 3V		1
22μf	T15V		2
32or47μf	E10V		4
47μf	T6V	±10%	1
100μf	E10V		1
220μf	E6V		1
1000μf	E6V		1
4700μf	E16V		1

Transistors		Quantity
MPSH05	or equivalent	1
BC182	,, ,,	7
BC212	,, ,,	2

Integrated circuits	
72741P	3
N5596K (Signetics)	1
NE555V	2
SN7400N	3
SN7404N	1
SN7408N	1
SN7413N	1
SN7420N	2
SN7430N	1
SN7432N	1
SN7447AN	6
SN7474N	2
SN7486N	1
SN7490AN	1
SN7492AN	1
SN7493AN	1
SN7412N	2
SN74157N	2
SN74164N	2
NE567V (Signetics)	1
LM309K	1

Displays	
DL747 or DL741 (Litronix)	6
TIL20	2

Miscellaneous	
Ferrite rod 7½in × ⅜ dia. F14 grade	Neosid
Aerial assembly	Denco
RM6 pot core assembly	Mullard
Transformer 4.5-0.4.5V (type 207-122)	RS Components
Meter (type MR100)	RS Components
Bridge rectifier (type REC41A)	RS Components
Plastic supporting pillars (type 63-1896-H)	Vero

Self-setting time code clock

3 — Alignment procedure

by N. C. Helsby, M.A., *University of Essex*

On completion, align the clock as follows.

Short the receiver input and adjust R_3 to give 4.3V at TP1. Remove the short and a signal should appear as soon as the a.g.c. has reduced the gain to the correct value. A voltmeter connected to the output of IC_3 will indicate signal strength by monitoring the a.g.c. amplifier output.

Adjust the aerial and T_1 tuning controls for maximum reading at this point, taking into account the slow response of the a.g.c. Note that the a.g.c. reference may be checked at the junction of $R_2 - R_3$ and should be about 2.9V. Similarly, the junction of $R_1 - R_2$ should be at about 3.6V. If the 5V supply is slightly high these values will be increased and the 4.3V should be raised accordingly.

Connect an audio amplifier to TP1, via a suitable capacitor, to check the overall noise level. Audible bleeps during the break in carrier may be heard using the tone generator.

In the decoder circuit, break the link on pin 4 of IC_{10} so that the timer runs continuously. If a timer/counter is available connect it to pin 3 of IC_{10}, and adjust R_{10} to give a period of 10ms. Alternatively, the output at pin 3 may be compared with 100Hz ripple on the power supply by adding the two signals and adjusting R_{10} for zero beats using an audio amplifier as shown in Fig. 16.

The code recognition circuitry may be set up using an audio oscillator and a pair of headphones. The oscillator is required to give a rectangular-wave output of about 4V pk to pk at 25Hz. The output should go from zero to +4V; if it does not it may be restored by means of a diode and capacitor. Disconnect the receiver from the decoder and connect the audio generator as shown in Fig. 17. Connect a link from the collector of Tr_3 to the base of Tr_5 so that the two collector resistors are shorted. Connect an audio amplifier or headphones to pin 8 of IC_{6b} via a 10kΩ resistor. Starting with R_8, adjust until the 25Hz output at pin 8 just ceases. Disconnect the link between Tr_3 and Tr_5 and with the same input signal, adjust R_7 so that the audio output just returns. This is the correct position for R_7 and, if an oscilloscope is available, the output at pin 8 should be high for 12ms under these conditions. If an oscilloscope is

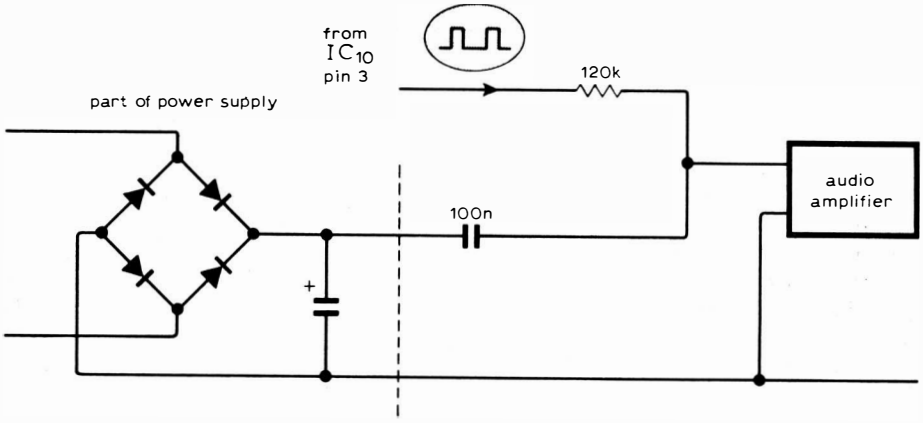


Fig. 16. Zero beat method of adjusting R_{10} avoids use of timer/counter.

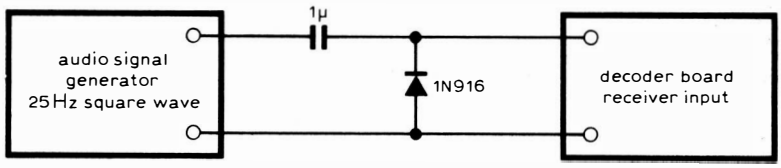


Fig. 17. D.C. restoration components ensure 0-4V input to code recognition circuitry.

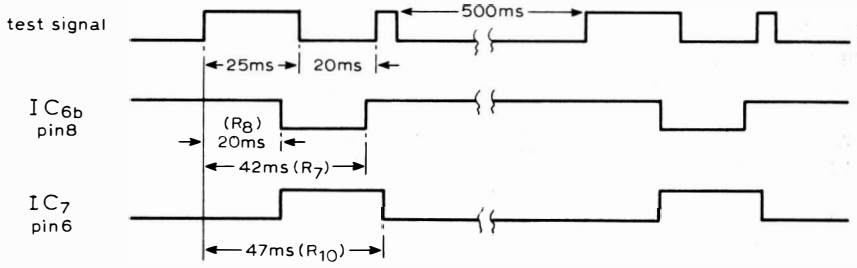


Fig. 18. Adjust R_7 and R_8 to give lower two waveforms, given test signal as shown.

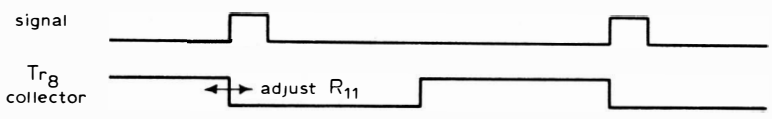
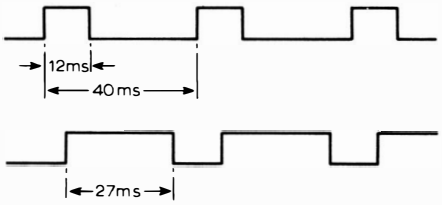


Fig. 19. Resistor R_{11} is adjusted for coincidence of positive and negative-going edges.



Waveforms on pin 8, IC_{6b} for correct setting of R_7 and on pin 6, IC_7 for a correctly-set R_{10}.

available continue to feed in the 25Hz test signal and set R_{10} to give a positive pulse length on pin 6 IC_7 of 27ms. If an oscilloscope is not available, adjust R_{10} to give the longest available pulse length. Disconnect the signal generator and connect the receiver output to the input of the decoder board. Decoding should proceed at each minute. To optimize the noise immunity, in the case where R_{10} was set, progressively advance it until decoding at the minute ceases, and then return it by a reasonable margin. The 25Hz oscillator continuously applied does not cause the decoder to trigger its clock, but it does so once each time it is switched to the input of the decoder.

As an alternative to the above procedure a test generator which gives the same waveform as the start of the time code may be constructed from monostables or standard test equipment. This waveform is applied at 500ms intervals and R_7, R_8 adjusted to give the waveform shown in Fig. 18 at pin 9 of IC_{6b}. The previous method using a 25Hz generator gives similar results. The timings shown allow for a margin of error in the transmitted code and the waveform shown will trigger the decoder clock every 500ms.

For the seconds counter and parity checker, remove the input seconds pulses by shorting the receiver aerial. Disconnect the link between R_{13} and pin 2 of IC_{16} and measure the voltage on pin 2 which should be around 3.5V. Apply the voltmeter between R_{13} and ground and adjust R_{12} to the same value as on pin 2. Reconnect the link and remove the short-circuit across the receiver aerial. Find the exremes of R_{18} at which the p.l.l. loses lock, as indicated by the out-of-lock l.e.d., and note the positions. Set R_{18} midway between these positions. (When lock is lost the indicator flashes on and off as the c.c.o. comes in and out of phase with the input signal). This adjustment must be made very slowly due to the long time constants involved. Adjust R_{11} so that the negative-going edge on the collector of Tr_8 is coincident with the positive-going edge of the received seconds pulses as shown in Fig. 19 (available on the edge of the seconds counting board). By mixing these signals through an audio amplifier, the exact coincidence point may be heard. This completes the alignment of the time code clock.

Printed circuit boards

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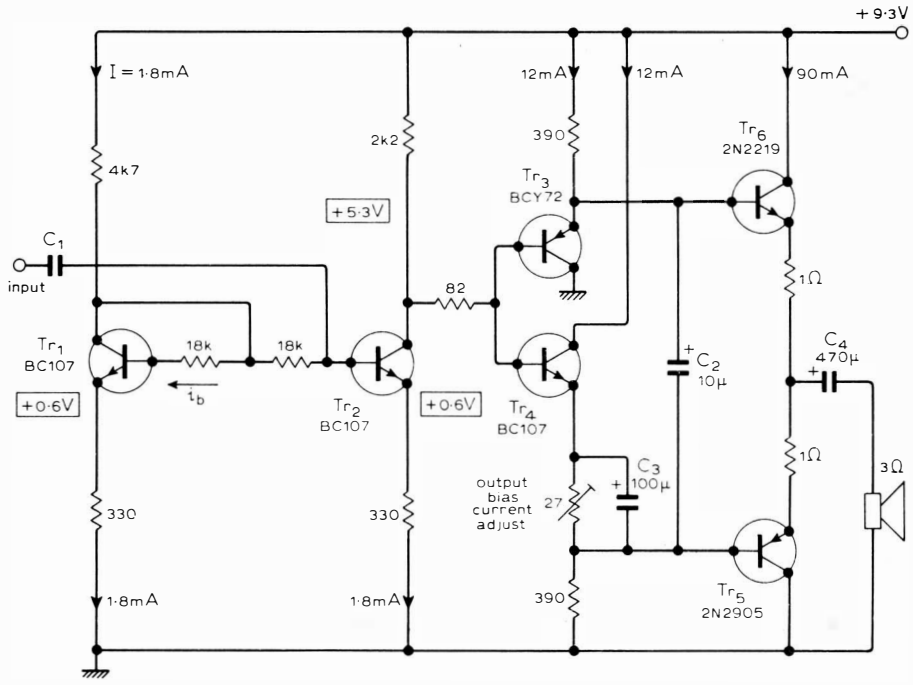
Circuit Ideas

Low voltage audio amplifier

This d.c. coupled amplifier does not include over all feed-back and is suitable for low supply voltage applications such as in-car entertainment. With a regulated 9V supply the circuit provides high quality sound at ample volume.

The double d.c. coupled push-pull emitter follower stages $Tr_{3, 4, 5, 6}$ provide base-emitter temperature corrected bias, as well as a low output impedance. Output bias current is adjusted with the 27Ω resistor. On positive transitions Tr_4 and Tr_6 are driven on, while Tr_3 and Tr_5 are cut off.



Capacitor C_2 couples the emitter of Tr_4 to the base of Tr_6 via C_3, so Tr_6 is driven hard on from the low impedance source of Tr_4. On negative transitions Tr_3 and Tr_5 are on, while Tr_4 and Tr_6 are off. Again, C_2 couples Tr_3 emitter to Tr_5 base. Thus, a symmetrical low output impedance is achieved on positive and negative transitions of an audio waveform. Driver transistor Tr_2 is designed to provide a temperature compensated bias and a maximum symmetrical voltage swing to the output stages.

Collector voltage of Tr_2 is set at approximately 5V d.c. so the emitter swing has to be contained within zero and one volt d.c. This means a low value for the emitter resistor and, therefore, a sensitivity to temperature variations. Temperature compensation is provided by a symmetrically biased transistor Tr_1, using collector to base negative feedback. www.keith-snook.info

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