Time by radio

A digital clock synchronized to a broadcast atomic time standard

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By combining an electric digital clock with a suitable radio receiver and a pulse discriminating circuit, it is possible to synchronize the clock to a selected time signal. The clock described here is designed to synchronize every minute to the signals broadcast from MSF Rugby, enabling it to be economically "slaved" to an atomic clock and display the nationally defined time scale to an accuracy of 1ms. Without the radio signals, the clock will run on its own internal quartz oscillator for several weeks before errors of a few seconds accumulate.

An independent and accurate clock (excluding portable atomic clocks) will usually depend on a quartz crystal which is chosen to suit the application. For example, a low frequency crystal (<100kHz) in a domestic situation should be stable to several parts per million, whereas a selected high frequency crystal operating at a closely controlled temperature can be stable, at no little cost, to parts in 10^7 per year. The frequency of oscillation of such crystals may in turn be checked directly against atomic clocks, or indirectly via the national and international frequency standards which are broadcast from various radio stations.

Although the rate of the crystal may be suitably uniform, it does not necessarily mean that the clock which it is driving is telling the correct time as this depends on the accuracy or manner with which the clock is set in motion. An example of this frequency checking approach has recently been given[1] where the temperature-controlled crystal was checked against the BBC 200kHz transmissions (the frequency of which is controlled by an atomic clock), but even so, it was acknowledged to be difficult to maintain the clock to within 3 seconds per year.

The alternative approach is to synchronize to specific impulses, a technique which has already been exploited with electromechanical clocks, but electronic clocks synchronized by "wireless" methods have advantages, including accuracy and portability.

The transmissions from MSF Rugby contain time markers, at 60kHz, taking the form of interruptions of the carrier as in Fig 1. The call sign is given twice in Morse code just before the hour, and corrections for the difference between UTCC and GMT are given each minute in the form of double breaks between seconds 01 and 15, the position and number of "emphasized" markers indicating the sign and magnitude of the correction in tenths of a second. The minute mark – of 500ms duration – is identifiably different in the signals and may be detected electronically for synchronization purposes.

Circuit operation

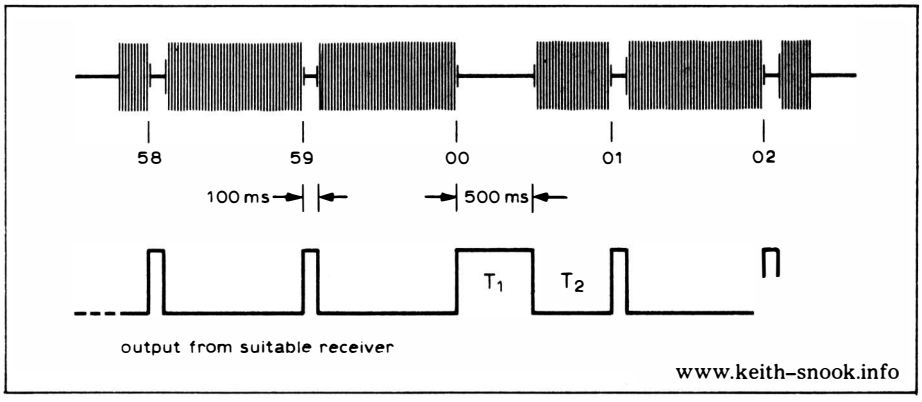
Briefly, the operation of the complete clock, shown in Fig. 2, is as follows. Assuming that the clock is already working, has been set manually to the nearest minute and is receiving the time signals, a special logic circuit detects the minute mark and "primes" the clock for synchronization at 01 seconds. At the instant this event is detected, the seconds display and part of the crystal dividing chain is set to zero and then restarted, and a subsidiary circuit restores the display to 01 seconds. If the clock was running up to 20 seconds slow then the synchronizing pulse would bring it forward; conversely, if up to 40 seconds fast it would be brought back to the correct time. Precautions are taken which ensure that any electrical interference cancels the process, and the clock continues uninterrupted and will synchronize after the next minute mark.

The central timekeeping element of the clock is a 2.097152MHz quartz crystal divided by 2^{21} to give 1Hz pulses. An output at 32Hz is also taken for the minute-mark detecting logic. C.m.o.s. integrated circuits are used to maintain the oscillator and carry out the division for a total dissipation of 3mW. The final 14-stage binary divider has a reset facility so that the counters may be set to zero and then released, the count being sufficiently far back so that the maximum error is about 0.06ms from the moment of release.

The digital clock part is conventional, using t.t.l. for further division, and non-multiplexed driving of seven segment l.e.d.-type displays. An input is available for zeroing the seconds and tens of seconds counters, and unless a synchronizing pulse is received at this input, or the dividing chain, the clock behaves as a normal digital clock with a crystal oscillator.

To receive the time signals, a straight t.r.f. receiver with a ferrite rod aerial is

Fig. 1. The form of time signals on 60kHz from MSF Rugby, prior to September 1974.



used. The rectified signal is inverted to give output pulses as in Fig. 1, and the bandwidth is made wide enough, together with a suitable gain setting, to ensure that the output follows the "r.f. off" transition to within 1ms. A.g.c. is not incorporated, because the received signal level is fairly constant, and also because an increase in gain when the transmitter is off would increase the sensitivity to noise.

A block diagram of the minute-mark detecting logic is shown in Fig. 3, and the method of operation is as follows. The output from the MSF receiver is applied to monostable A and gates B and C, the monostable having a period t_1, where $t_1 < 1$ms for a synchronizing accuracy of better than 1ms. On arrival of the minute mark at 00 seconds, the monostable is triggered and in turn resets the binary counters and the RS flip-flops D and E as shown; for the remainder of the pulse (period T_1, Fig. 1) the gate B is opened, passing the 32Hz pulses to the four-stage binary counter F, flip-flop D being set after a count of 15 has accumulated. (Any interference detected during this period causes a reset and the process is abandoned.) The output from flip-flop D, together with gates C and G, pass the 32Hz pulses to counter H when period T_2 (Fig. 1) commences. As before, flip-flop E is set when a count of 15 has accumulated, and again any interference during the count will cause a reset.

The system is now "primed" and ready to pass a reset pulse to the counters at 01 seconds. This is achieved by passing the reset pulse through gate I, which is possible only when both flip-flop E is in the required state and the third input is set to logical 1, either manually or automatically, by the clock. In order to reduce further the risk of setting the clock to a burst of interference after initial synchronization, this latter facility may be used so that the clock itself will only permit synchronization between seconds 58 and 02.

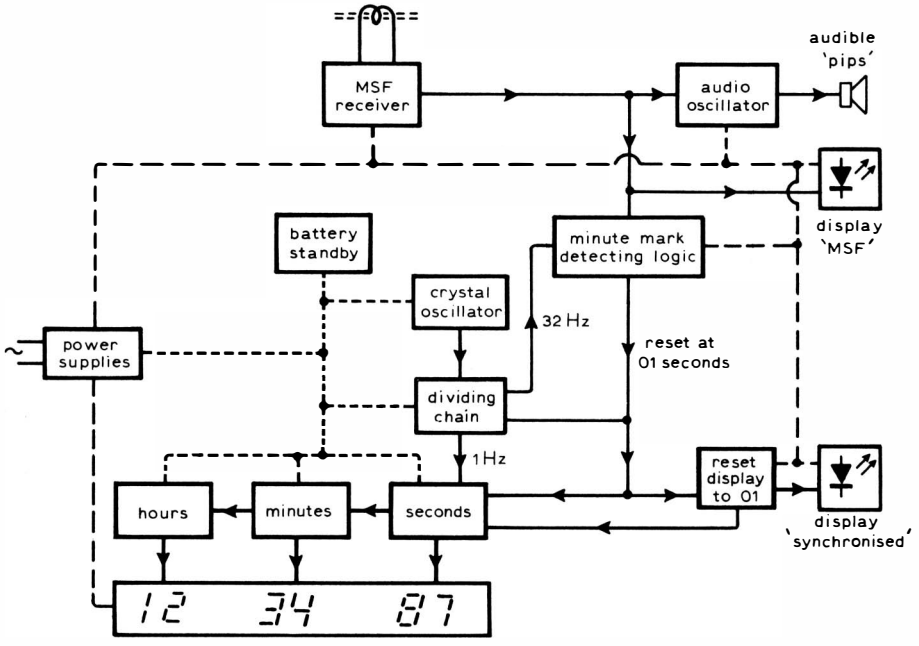
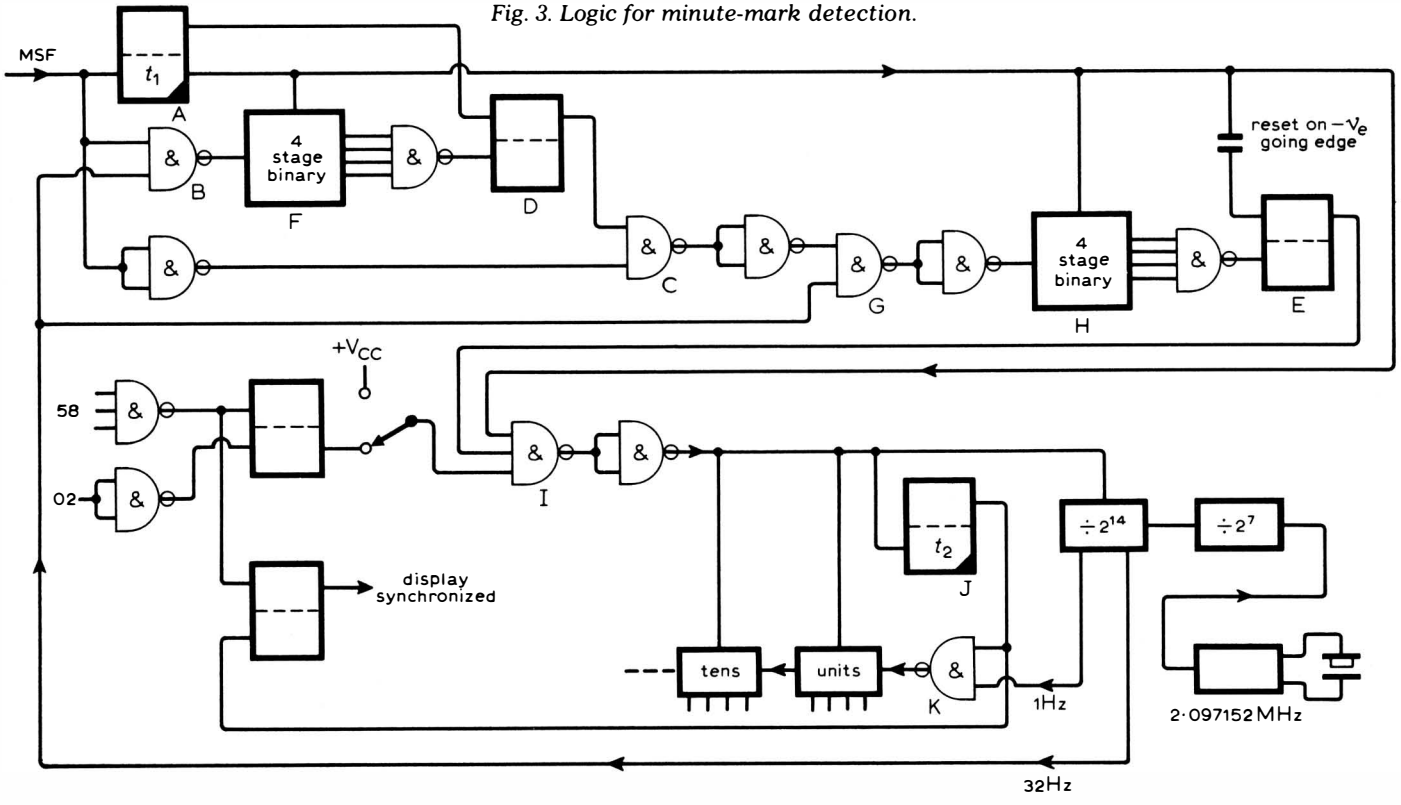


Fig. 2. Block diagram of the complete instrument. Standby battery powers the oscillator and counters only, as shown by dotted line.

In the "primed" state the circuit now awaits the arrival of time marker 01, and when this occurs a reset pulse is transmitted to the oscillator dividing circuit and the seconds counting stages of the clock, causing the clock to display 00 seconds, and monostable J changes state. This monostable has a period $t_2 > t_1$, and at the end of t_2 the output of gate K returns to logical 0 causing the display to read the correct time, i.e. 01 seconds; t_2 is sufficiently brief so that any flicker in the display is undetectable. The output of the monostable also resets the separate display indicating that synchronization has taken place.

The operation is such that the system is "primed" after counting 15 of the 32Hz pulses during period T_2 and therefore exposed to the radio signals for a waiting period of about 30ms. Any interference before the seconds marker could put the clock in error by up to 30ms, but this risk could be reduced by changing the 32Hz pulse train to some higher frequency and using more counters to count up to say 495ms,

Fig. 3. Logic for minute-mark detection.



when the "prime" interval would be about 5ms.

As far as can be determined the clock works perfectly in a domestic environment, but a further refinement to ensure foolproof minute-mark detection could take the form of another counter stage following the first four-stage binary. This could be arranged to cause a cancel if a count of 17 were accumulated, indicating that period T_1 was longer than 500ms and therefore not genuine.

The performance of the clock may be summarized in the following remarks. After initial setting it will detect the minute mark and synchronize at 01 seconds to an accuracy of 1ms; it will similarly synchronize at each successive minute; positive or negative leap seconds are automatically followed; a light shows that the clock is in the synchronized condition; any radio interference detected during the minute mark and the next 470ms causes the synchronizing process to be abandoned for that minute; once synchronized, the clock may be set so that synchronization is possible only between seconds 58 and 02; if the clock is so set, the quartz crystal will enable the clock to be without the radio signals for about 2 weeks before drifting "out of lock"; a battery standby maintains the oscillator and dividing circuits if disconnected from the mains, and on reconnexion the correct time is displayed and synchronized after the next minute mark.

It is quite feasible to synchronize a clock by similar means to other time signals, either from other low frequency transmitters, such as Switzerland's HBG (75kHz) or Germany's DCF 77 (77.5kHz), or the "six pips" in domestic

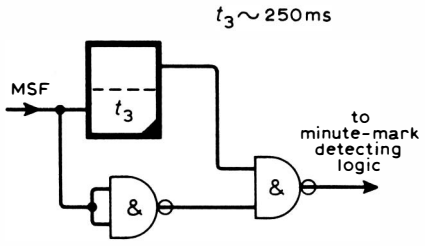


Fig. 4. Pulse-stretching logic to maintain independence from the new NPL time code.

services[2], all of which have different but identifiable components in their signals.

The clock had been operating satisfactorily since October, 1973, until mid-September 1974 when the National Physical Laboratory introduced a modification to the time signals. The purpose of this change is to broadcast a time code of GMT hours and minutes, so that each minute may be electronically identified without the use of a separate clock or counting from the hourly call sign. The code consists of a number of 10ms pulses containing the time information in b.c.d. form within the first 200ms of the originally blank part of the minute marker[3] (period T_1, Fig. 1). Unfortunately, as a consequence of the design, my clock rejected this information as interference! However, by using a pulse stretcher as in Fig. 4, and inserting this between the radio and the minute mark detecting logic, the time code may be blanked out so that the clock synchronizes each minute as before.

Fig. 5. Digital clock circuit diagram.

It is worth emphasising the differences between these two schemes. The NPL time code enables one to have a *radio* with a decoder which (assuming no problems with interference) gives the nationally defined time, and the ability to switch the "clock" off say, in the evening, and then obtain the correct time within a minute of switching on the next morning. Conversely, if the transmitter goes off the air, as it does for 4 hours per month, the time is not available. The system described here, on the other hand, is a *clock* which is able to synchronize by radio the seconds and part of the oscillator dividing chain to within 1ms of the time scale. This method has a greater degree of independence, in that it will continue to give the time without the radio signals. Clearly, a future system could combine the advantages of the two separate approaches.

Construction

These notes and accompanying circuit diagrams represent the clock in its finished form, and as such contain a partial record of its development. The clock is capable of further refinement, either in design or by the use of bought out items, and these notes are intended to give general information, rather than give a detailed circuit description and act as a practical or constructional guide.

Digital clock. This circuit, shown in Fig. 5, was constructed on a 5 × 3¾in Veroboard, permitting reasonable spacing between the integrated circuits. The displays were mounted at right angles

to the plane of the board along one edge by wiring the sockets in a wire frame and bridging the 150 current-limiting resistors directly from the 7447s, this resistor value being as given in a Hewlett Packard data sheet for a current of about 22mA per segment. Setting of the clock is achieved with a three-position switch on the rear panel by routing to the minute count, either 1Hz or 32Hz pulses, enabling a fairly rapid run through of the hours (32Hz), to be followed by a slower minute advance, and normal operation. Using this size of board and layout and components as shown in the diagram, no problems were due to interference were experienced. Some power supply connexions have been omitted in the diagram to avoid repetition.

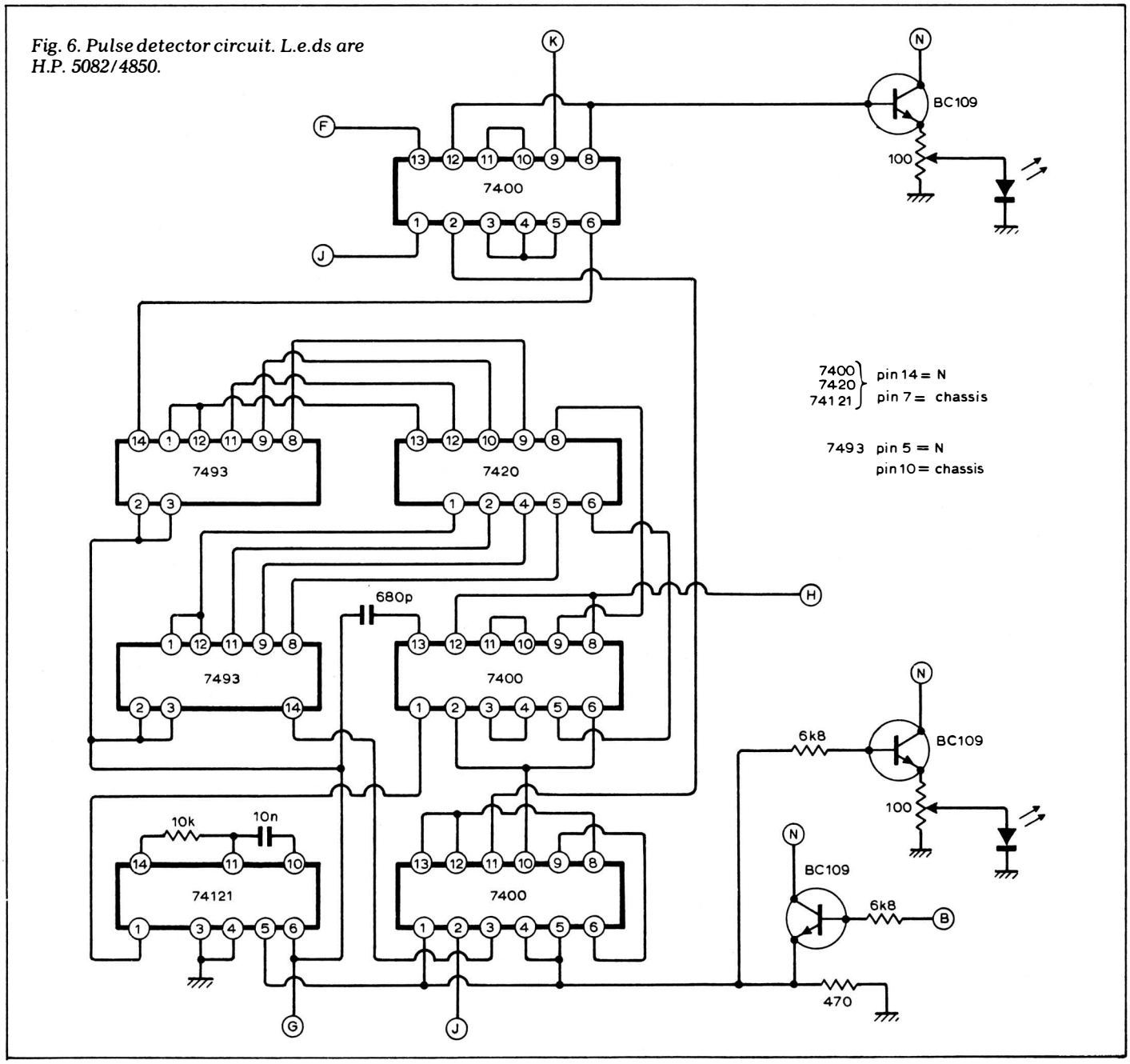
Pulse detecting logic. A 5 × 3¾in Veroboard was also used for the circuit of Fig. 6 and the board was bolted to metal strips attached to the clock board, so that all the digital circuitry was in effect on one large panel, 7½ × 6 inches in size.

In order to permit synchronization at any time during the minute, a switch on the rear panel may be put open circuit (=1 input to the triple-input gate 7410); with the switch closed a 1 is available only during seconds 58 — 02, restricting synchronization to this time slot. Note that the "synchronized" l.e.d. goes on at 58s and off if synchronized, but remains on if synchronization does not take place.

Crystal oscillator. The 2.097 152MHz crystal was purchased from the McKnight Crystal Co., Southampton, and the oscillator circuit in Fig. 7 is based on the data given in the RCA Application Note ICAN 6086 — "Time-keeping advances through COS/MOS technology." Frequency setting was achieved by monitoring at pin 12 of the seven-stage binary, CD4024AE, thereby avoiding loading of the oscillator. The 18kΩ and 6.8kΩ resistors in the V_{DD} leads were left in the circuit after current/voltage experiments. A 3¾ × 2in Veroboard was used for the oscillator and divider chain, the whole being mounted in a metal box. The reset control could be operated manually to stop the oscillator and clock, for either releasing the clock near a given time signal, or demonstrating the synchronizing abilities of the clock after having been set wrongly for a number of seconds.

Radio receiver. The 60kHz radio waves are picked up on an external tuned ferrite-rod aerial, the stepped down output being fed down a 2m length of coaxial cable to the receiver. The length of cable is not critical, 50m having been used with only a slight effect on the tuning. Aerial dimensions, number of turns, and value of tuning capacitor are also not critical, but a signal generator is useful in initially finding resonance. Similarly, situation is not critical, a safe and convenient place being floor or

Fig. 6. Pulse detector circuit. L.e.ds are H.P. 5082/4850.



ground level, providing the aerial is not too near a ring main, or other source of switching transients, etc.

A straightforward t.r.f. amplifier, followed by a diode rectifier, d.c. amplifier and Schmitt trigger, comprises the complete receiver as shown in Fig. 8. The r.f. stages are not conventional, and damping resistors were used at an early stage in the design to ensure wide bandwidth; indeed, in the presence of strong signals the tuned amplification could be dispensed with. The circuit shown has a bandwidth of about 400Hz and, with a low gain setting, gives a 1 output within 1ms of the r.f. off transition. Constructionally, care had to be taken to prevent oscillation by earthing unused strips on the Veroboard, and mounting in an aluminium box.

Audio oscillator. An LC oscillator was chosen to give a reasonably stable 1kHz sinusoidal waveform. Although the "modulator" gives a slight click for each "on," this system gives quite adequate pips. Fig. 9 shows the circuit diagram.

Pulse stretcher. In order to maintain independence from the new NPL time code (introduced in September, 1974) a pulse stretcher is necessary to override the code which ocurrs during the first 200ms of the originally blank part of the minute mark. Fig. 10 shows the relatively simple modification, which was included on the same board as the pulse detecting logic, together with some additional power supply decoupling, and consists of a monostable and gates interposed between the MSF input buffer transistor and the pulse detecting logic; the monostable timing resistor is about 14kΩ for C = 25μF.

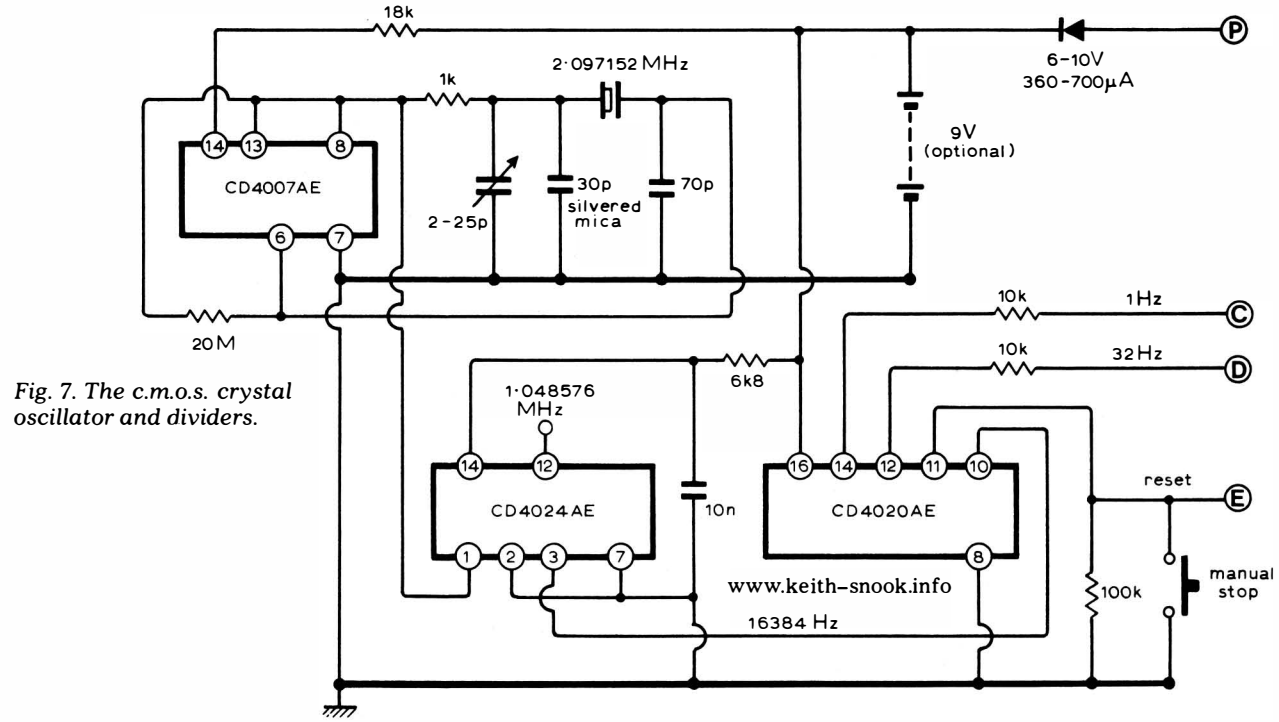


Fig. 7. The c.m.o.s. crystal oscillator and dividers.

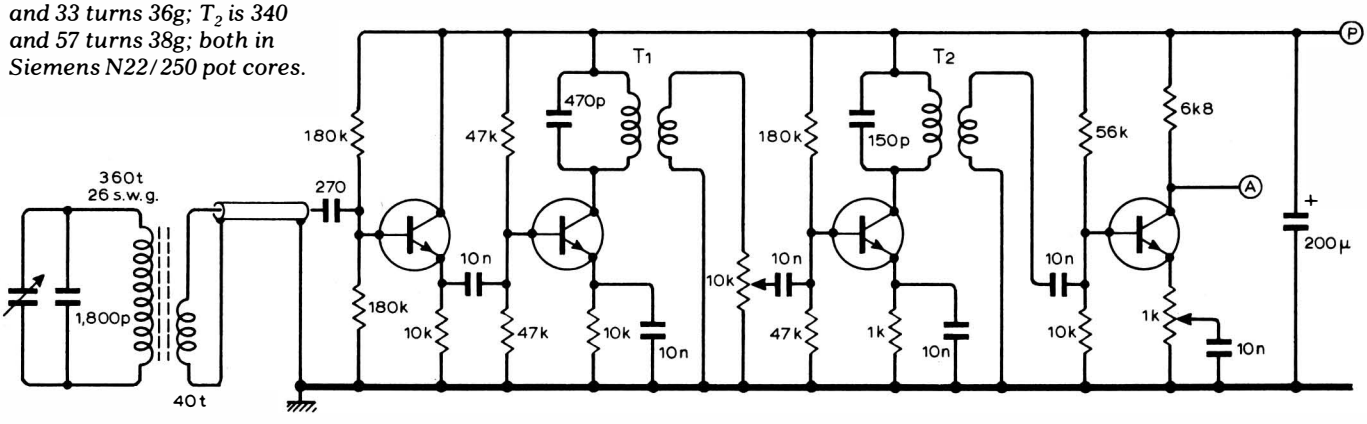


Fig. 8. 60kHz radio receiver and pulse shaper. T_1 is 200 and 33 turns 36g; T_2 is 340 and 57 turns 38g; both in Siemens N22/250 pot cores.

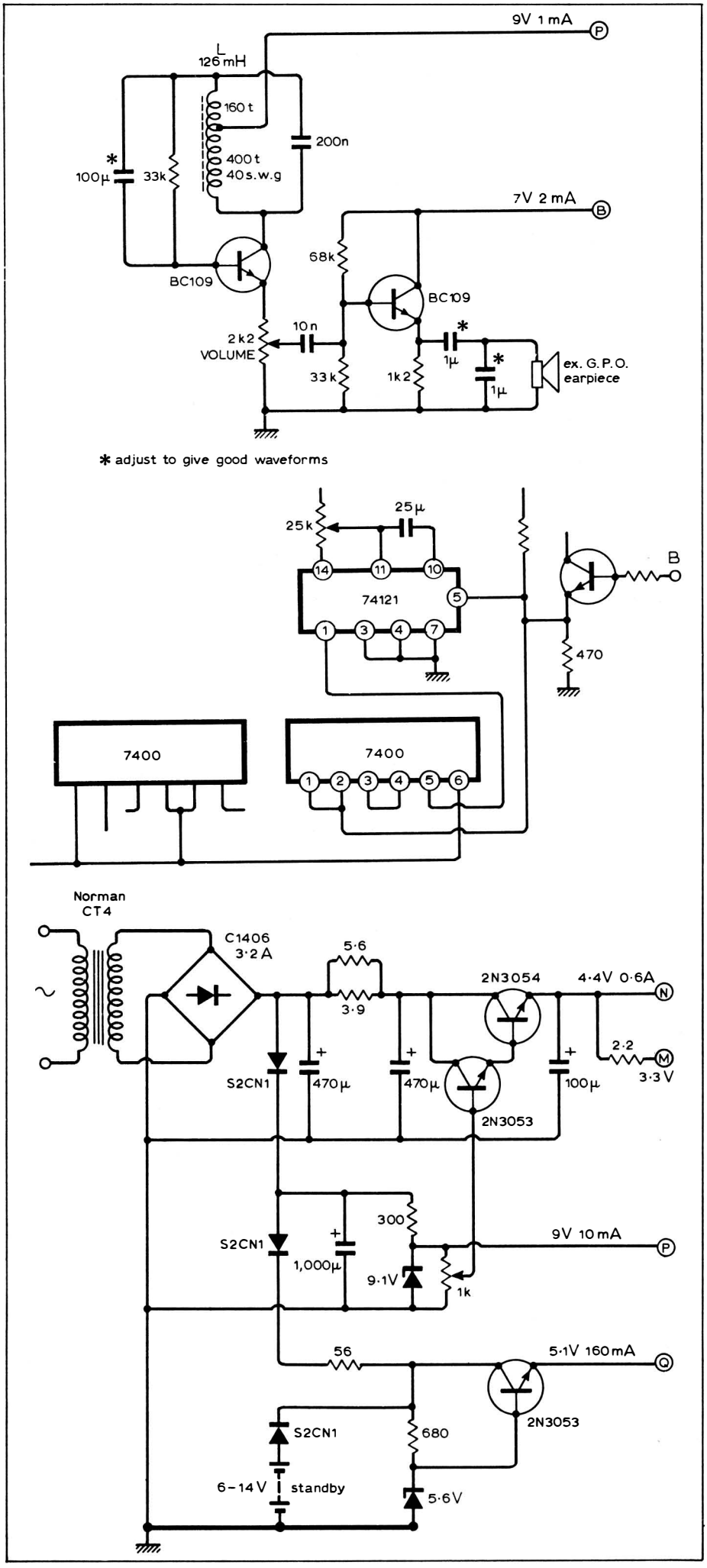


Fig. 9. The 1kHz oscillator is in Siemens N28/400A pot core.

Fig. 10. Pulse-stretcher circuit.

Fig. 11. Power supply with battery standby. Rectifier and diodes are Electrovalue types.

Power supply. This was developed specifically to give battery standby to the "heart" of the clock, i.e. the crystal oscillator and the clock divider chain, and it is very satisfying to move the clock from one location to another and display the correct time as soon as it is plugged into the mains! The circuit is that of Fig. 10.

Originally, the supply was designed for the relatively heavy current consumption of 1A for l.e.d. displays requiring 22mA per segment, but the more efficient type finally used was set for about 12mA per segment by simply lowering the output volts and inserting a series resistor to avoid changing all the 150Ω resistors. When the mains supply is turned off the l.e.d.s and drivers go off without affecting the timing.

The clock logic is driven from a separate 5V supply with a battery standby, a PP9 giving nearly an hour of continuous reserve: an external socket gives extended capability from a 12V lead-acid battery if required. The crystal oscillator also has its own battery standby — a PP7 — but this is partly for historical reasons, as when finished at an early stage, the oscillator was left running continuously.

Case. For the case, the attractive Vero D series was used, type 81CD-1U-3 and 8FP-1U-19 front panel. A particular advantage of this (large) case was that the lower panel on which the various circuits and boxes could be generously spaced out, could be unscrewed. A minimum number of items were included in the front panel — an aperture with a red plastic filter to improve the contrast of the displays, the two l.e.d.s showing the presence of MSF and state of synchronization, and pip volume control — the remaining switches and sockets being mounted on a specially included rear panel.

References

1. J. F. K. Nosworthy. "The Cranleigh School quartz-crystal digital clock and ten-millennium calendar," *Horological Journal*, Vol 116, 3-10, October 1973, and *Wireless World*, Vol. 80. No. 1463, July 1974 *et seq.*
2. G. C. Baggott, private communication.
3. B. R. Swabey, National Physical Laboratory. www.keith-snook.info