Time-code receiver clock — 1

An accurate and automatic digital time-piece

by A. F. Cross, B.Sc.
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Last year time code transmissions started from Rugby on 60kHz, offering a new approach to accurate time-keeping in the UK. This article describes a 24-hour digital clock of flexible design, based on the Rugby signal.

Many designs for digital clocks have been published, but generally they have had two drawbacks; they require an accurate internal frequency source and manual setting. While the first problem may be solved, at a price, the second usually involves the GPO speaking-clock. This design was aimed at producing a relatively inexpensive time-piece capable of keeping correct time without regular checking. The usual mains-derived reference, whilst having a low long term frequency error, exhibits a high short term variation, with the result that a clock can be in error by several seconds at any time. On the other hand, a local crystal reference will exhibit an accumulating long term error.

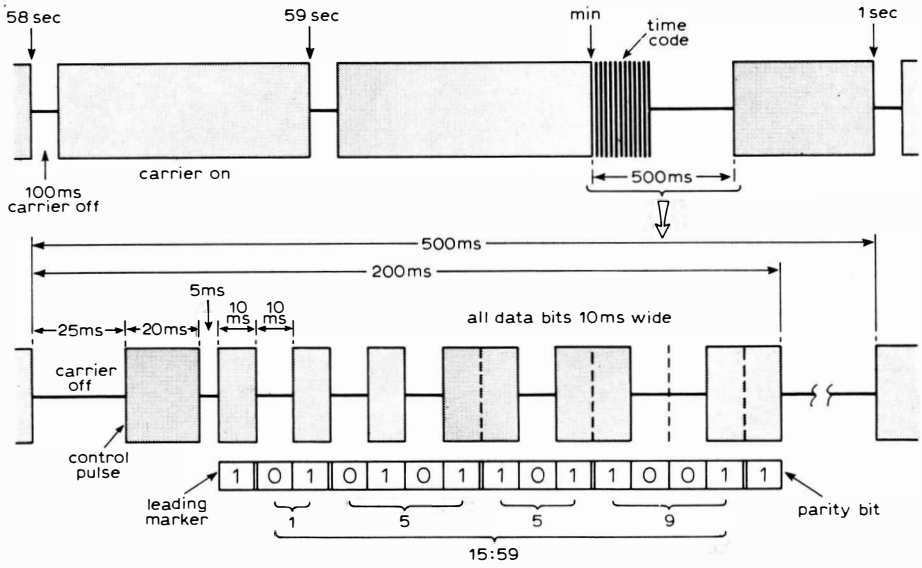
The clock to be described uses a crystal oscillator and divider chain. Checking and setting of the clock is provided automatically by a received time code.

Transmission

The National Physical Laboratory has been controlling the transmission of 1s pulses radiated on 60kHz from the GPO transmitter at Rugby. In 1974 a data code was added to the signal to give the exact time of day. The carrier is on-off modulated, as shown in Fig. 1. The one-second intervals are indicated by the start of a 100ms break in carrier, and the minute by a 500ms break. The data has been added to the 500ms break. The 20ms control pulse indicates that data is to follow, which comprises a leading 1 followed by thirteen data bits for hours and minutes. The data is followed by a parity bit which checks that the data has been correctly received.

The carrier, and hence the pulse timing, is based on a rubidium reference at Rugby, which is compared with a caesium reference at the NPL Teddington; the deviation is usually in the order of 1 in 10^{11}. The clock uses the timing of the code to resynchronize the reference divider, and the data to check and correct the displayed time. Several checks are carried out on the time code before it is allowed to influence either internal timing or displayed time. The transmission is normally maintained twenty four hours a day, except for five or six hours on the first Tuesday of each month to allow for maintenance. The clock will free-run during this period and the accumulated error (a fraction of a second) will be eliminated when the code is again received.

Fig. 1. On-off modulation of the 60kHz carrier – one-second intervals are indicated by the start of a 100ms break, and the minute by the 500ms break.



Initially, consideration was given to using the one-second received pulses to clock the seconds display. This method has problems because interference can cause multiple clocking, and other information, which is transmitted during the minute, must be discriminated against. It was decided for overall simplicity to derive the 1Hz signal from the reference divider. Although the transmitted code is always GMT, or more precisely UTC (Universal Co-ordinated Time), the facility for switching the display to BST manually has been provided. A further feature of the clock is that it will follow the internationally agreed time-scale corrections, often referred to as the leap-second. This is a one-second correction which is made to all standard clocks to maintain tracking between the precise atomic standard and the astronomic time scale. The correction is made every 12 or 18 months as required *(Wireless World,* June 1971, p.276). A free-running clock, no matter how accurate, cannot carry out this adjustment automatically.

System operation

The block diagram in Fig. 2 shows the interconnexion between the circuit functions, each of which may be constructed independently. The circuit may be considered in two sections; a free-running clock, and a receiver plus control logic. The clock comprises the hours, minutes and seconds dividers and displays, the crystal oscillator, and the 5-decade reference divider. These sections together will operate as a normal digital clock, except that no manual setting facility is provided.

The receiver amplifies and demodulates the 60kHz signal which is then passed to the time code register section. When a control pulse has been detected a 100Hz clock loads the serial data into the shift register. When the register is full, clocking ceases and, if parity is correct, a data strobe pulse is generated. The data in the register is applied to the 13-bit comparator, which also receives data from the hours and minutes display-dividers. An output from the comparator to the control logic indicates whether the display-dividers agree with the received data. Upon receiving the data-strobe signal from the time-code register, and a comparison error signal from the comparator, the control logic initially assumes that the error is in the received code. If, however, two consecutive received data words both give an error signal, the control logic acts to correct the display-dividers. This is achieved in less than 15ms by fast-clocking the hours and minutes-dividers at 100kHz until the comparator gives the no-error signal. In normal operation the received code agrees with the contents of the hours and minutes display-dividers. The control logic then resets the seconds-divider, which should be reading zero, and resynchronizes the 5-decade divider, which is normally a correction of less than 1ms. The outputs of the hours-divider pass through the GMT/BST converter before driving the display logic. With the converter set to GMT there is no effect on the hours data; when set to BST, a one hour correction is made to the display.

Clock options

It is possible to simplify the clock by omitting certain functions. The simplest circuit would comprise the receiver, the time-code register and the four-digit display logic. Such a clock would display GMT hours and minutes. A 1kHz signal is required to control the clock generator, but its accuracy need only be about ±1% and a 555 timer would be suitable. Retaining three decades of the divider chain, and improving the accuracy of the 1kHz clock to about ±0.1% would produce a 1Hz signal for clocking a seconds-divider. The 3-decade divider would be resynchronized with the data-strobe signal, which would also reset the seconds count. In the absence of a carrier these simplified clocks would cease to function correctly because there is no display counter. This also means that there is little protection against incorrect data; once a control pulse has been detected the display will show the contents of the shift register, even it it is wrong. The parity signal can, however, light a warning indicator. Also, if a control pulse is not recognised, the display will not update, but continue to show the previous time code. Even with these limitations, a simplified version of the clock can still find useful applications where an occasional time check is required and a continuous reliable readout is not necessary. The GMT/BST converter may be included or omitted as required.

Circuit operation

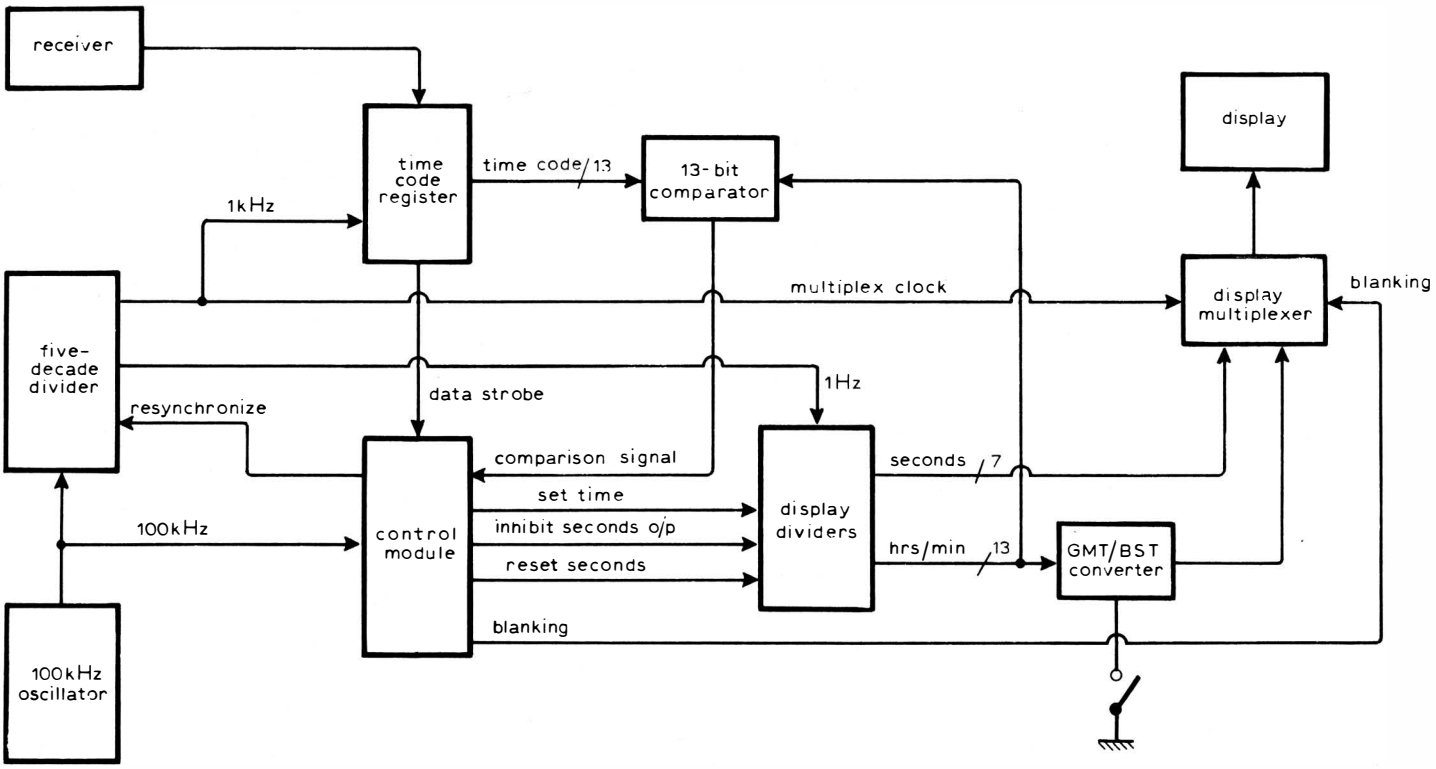
The units of seconds, minutes and hours each use a 7490 decade counter, and the tens-of-seconds and minutes use a 7492 divide-by-12 as shown in Fig. 3. With the most significant bit ignored, (output D) the device divides by 6 in binary sequence. The tens-of-hours divider is provided by a 7473 dual JK flip-flop, and the 24-hour reset is provided by a D-type flip-flop.

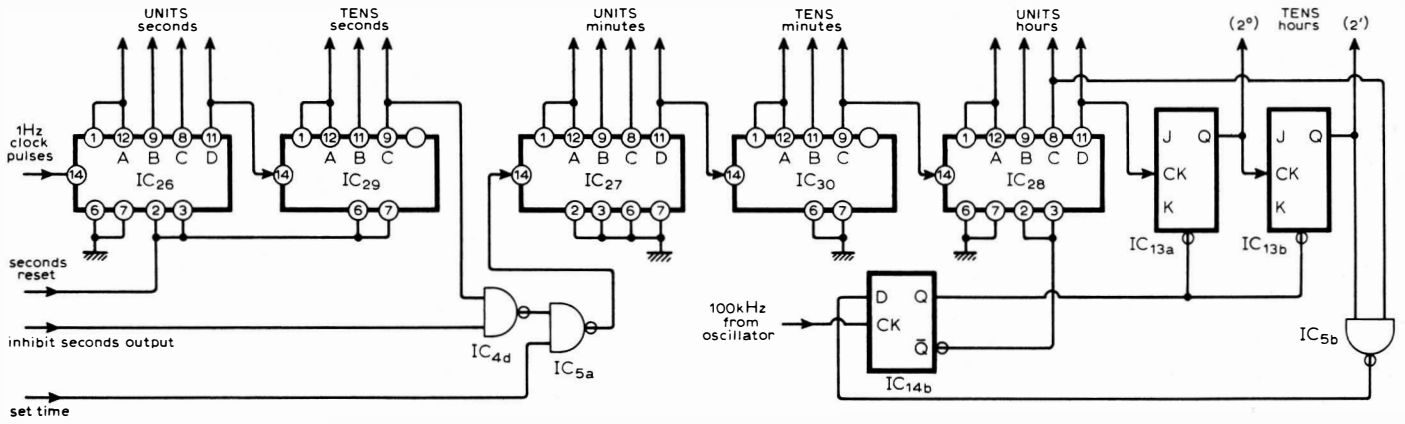
When a count of 24 exists in the hour-dividers a logic 0 is applied to the flip-flop via NAND gate IC_{5b} which is connected to the appropriate divider outputs. Because the D-type is clocked at 100kHz, the 0 on the D input will be clocked within 10μs, which sets the Q output to 0 and the $\bar{Q}$ output to 1. The Q output provides a low reset to the JK flip-flops for tens-of-hours; the logic 1 on the $\bar{Q}$ output provides the required high reset on the hours-units-divider. The D input now changes back to a 1, but the D-type does not change until the next clock pulse. Thus a 10μs reset pulse to the hours-divider is ensured.

The NAND gates IC_{4d} and IC_{5a} between the seconds and minutes-dividers provide the facility for injecting fast clocking pulses into the minutes and hours-dividers for time setting. In normal operation these gates have no effect, and the output pulses from the tens-seconds divider pass to the clock input of the units-minutes divider. When the fast-set condition is operating, the inhibit-seconds ouput signal goes low, thereby forcing the output of gate IC_{4d} to logic 1. Pulses at 100kHz appear on the set-time input of gate IC_{5a} which are then inverted. Thus the hours and minutes count is advanced at 100,000 steps per second. The maximum setting time is determined from the time taken to clock the dividers through 24 hours i.e. 14 4ms.

Fig. 2. Block diagram which may be considered as two sections – a free running clock, and a receiver plus control logic.

The 5-decade divider is shown in Fig. 4 and comprises five 7490 i.cs. Besides





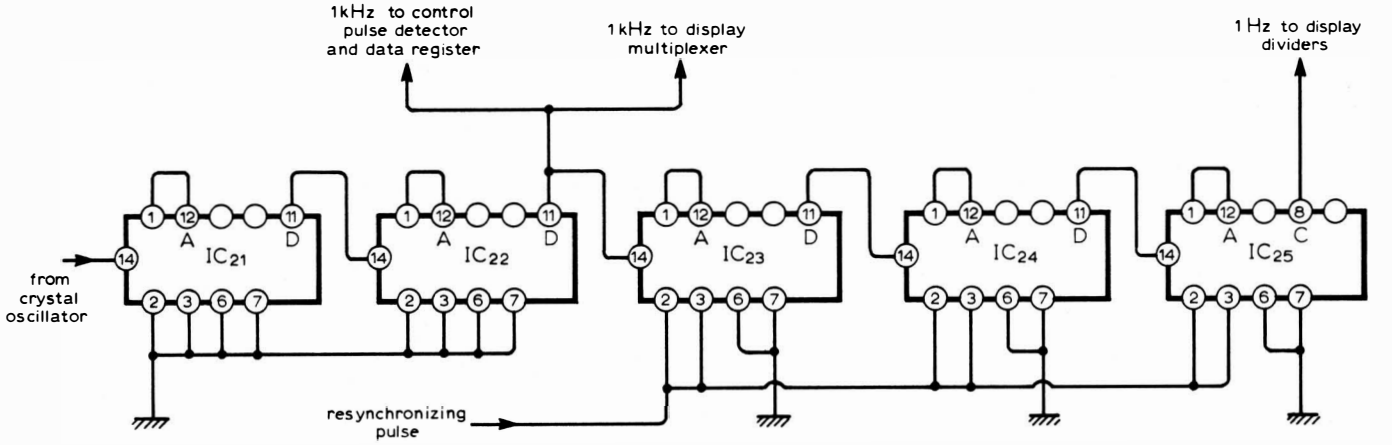
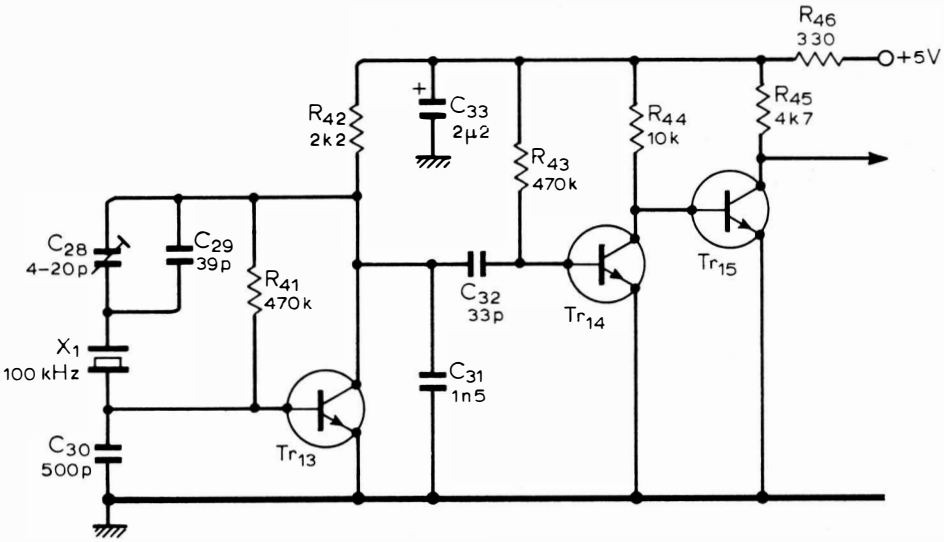


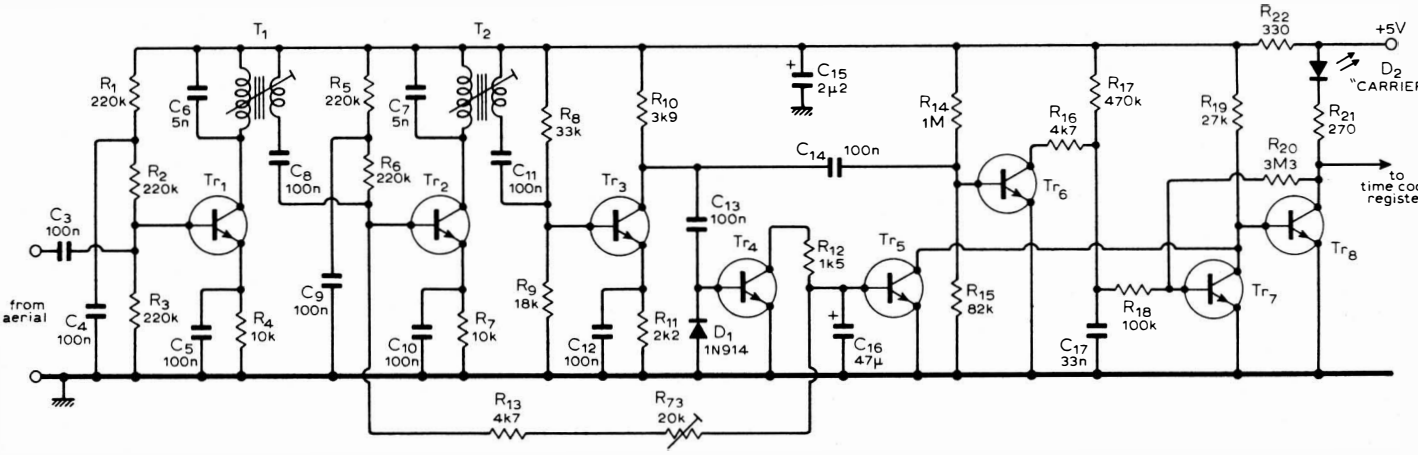
Fig. 3. (top) Display dividers — seconds, minutes and hours each use decade counters and the tens of seconds and minutes use divide-by-12s.

Fig. 4. (above) Five-decade divider. Besides providing the 1Hz output for clocking the display dividers, it also provides 1kHz for the time-code register.

Fig. 5. (right) Oscillator circuit incorporating a two transistor buffer to produce a t.t.l. compatible output at 100kHz.

Fig. 6. (below) Receiver and demodulator circuit. A.g.c. is applied over the second and third stages.





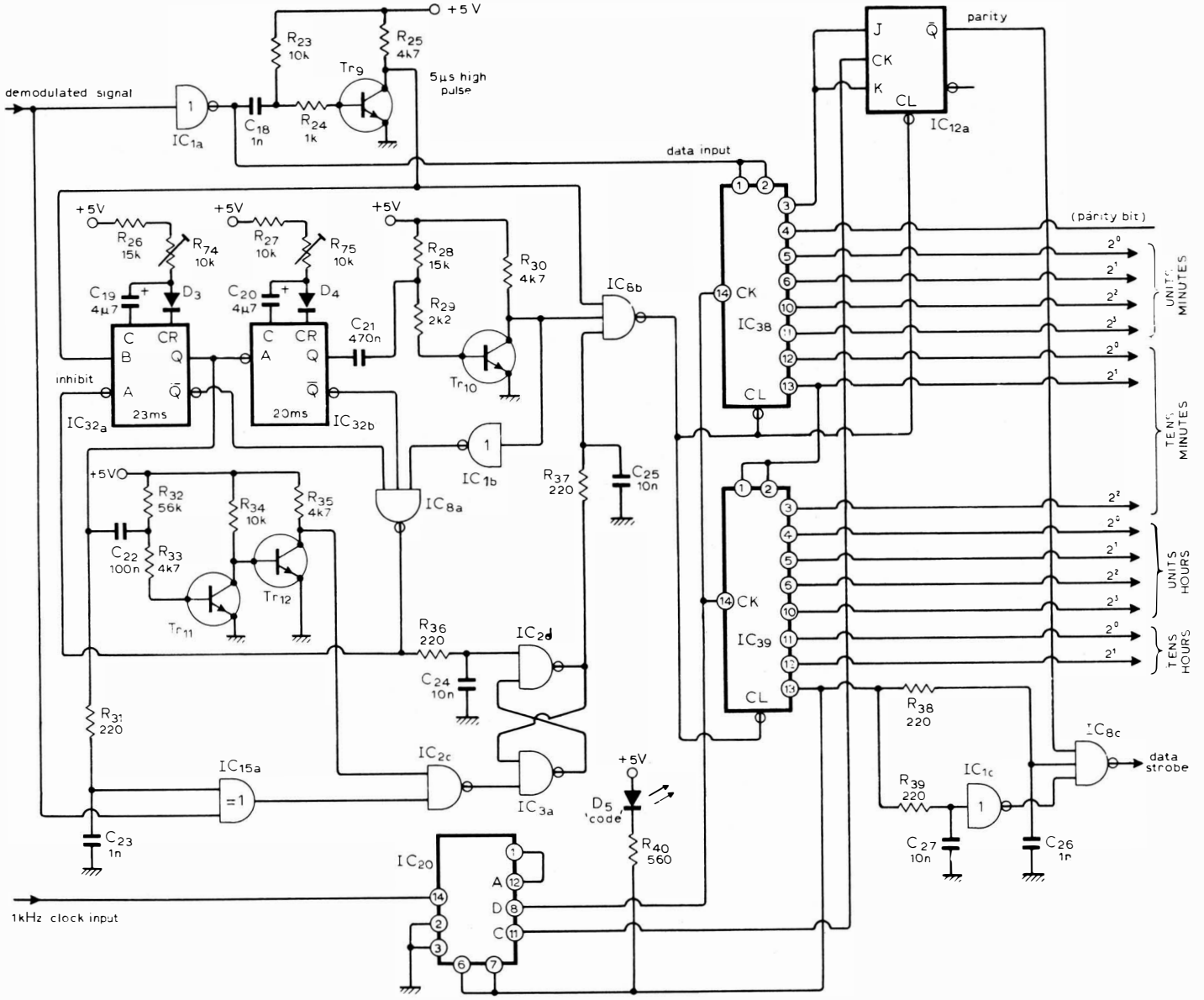


Fig. 7. Time-code register – takes in the demodulated signal, detects the control pulse and stores the incoming time code.

Truth table for decade counter

	D	C	B	A
Reset at 0.2s	0	0	0	0
State at 0.3s	0	0	0	1
State at 0.4s	0	0	1	0
State at 0.5s	0	0	1	1
State at 0.6s	0	1	0	0
State at 0.7s	0	1	0	1
State at 0.8s	0	1	1	0
State at 0.9s	0	1	1	1
State at 1.0s	1	0	0	0
State at 1.1s	1	0	0	1
State at 1.2s	0	0	0	0

Box: 1-0 transition provides clocking output at end of second.

providing the 1Hz output for clocking the display-dividers, it also provides 1kHz for the time-code register, which in turn derives the 100Hz data clocking pulses. The 5-decade divider is resynchronized by resetting the last three dividers. The resetting pulse from the control logic appears at the end of the received data word, which is about 200ms after the beginning of a second as shown in Fig. 1. Conventional setting to zero would therefore result in the clock being permanently 0.2s slow. However, Truth Table 1 for the decade divider reveals that, although the D output goes low one second after the zeros reset, the C output does so after 0.8s. If, therefore, the C output is used to clock the seconds-display dividers, the indicated time will be correct to within about 5ms.

The oscillator circuit in Fig. 5 is quite conventional. A two transistor buffer is added to produce a t.t.l. compatible output which operates at 100kHz. When the Rugby transmitter is switched off for maintenance, the crystal oscillator is required to hold the correct time to an accuracy of about 5 parts per million. This can be achieved by a simple oscillator, over a restricted temperature range but, if greater accuracy is required, a temperature-compensated oscillator should be considered.

The receiver, see Fig. 6, uses a ferrite rod aerial, followed by three stages at r.f., the first two being tuned. Automatic gain control is applied over the second and third stages and a simple transistor demodulator is employed followed by d.c. amplification to provide a t.t.l. compatible output. At low signal levels a muting circuit inhibits the demodulator output. The r.f. stages are conventional and require little explanation. The tuned transformers are not critical and the originals were hand-wound. Transistor Tr_4 is the level detector for the a.g.c. circuit. Signal peaks exceeding the base-emitter threshold voltage will result in Tr_4 discharging the a.g.c. reservoir capacitor C_{16}. This reduces the base bias voltage to Tr_2 which reduces the gain of the second stage. With a.g.c. operating, the signal at the collector of Tr_3 is between 600mV and 800mV peak-to-peak. The a.g.c. voltage is detected by Tr_5 and no-signal or a weak signal will result in an increase in a.g.c. voltage. When this voltage turns Tr_5 on the output of the demodulator is inhibited. To allow for differing transfer characteristics and variations in signal strength, a potentiometer (R_{73}) in the a.g.c. feedback line may be used to vary the level of signal at

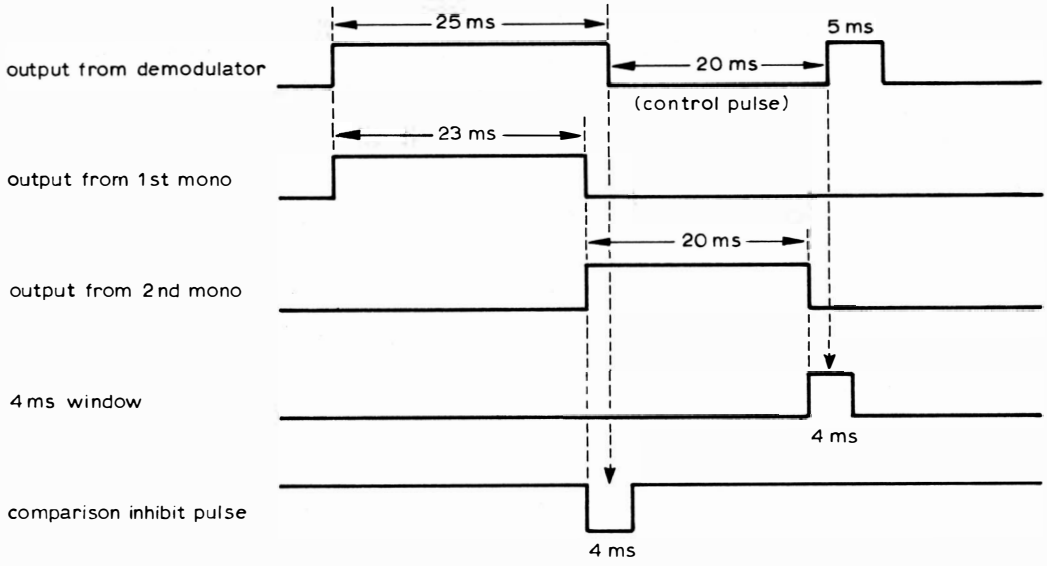


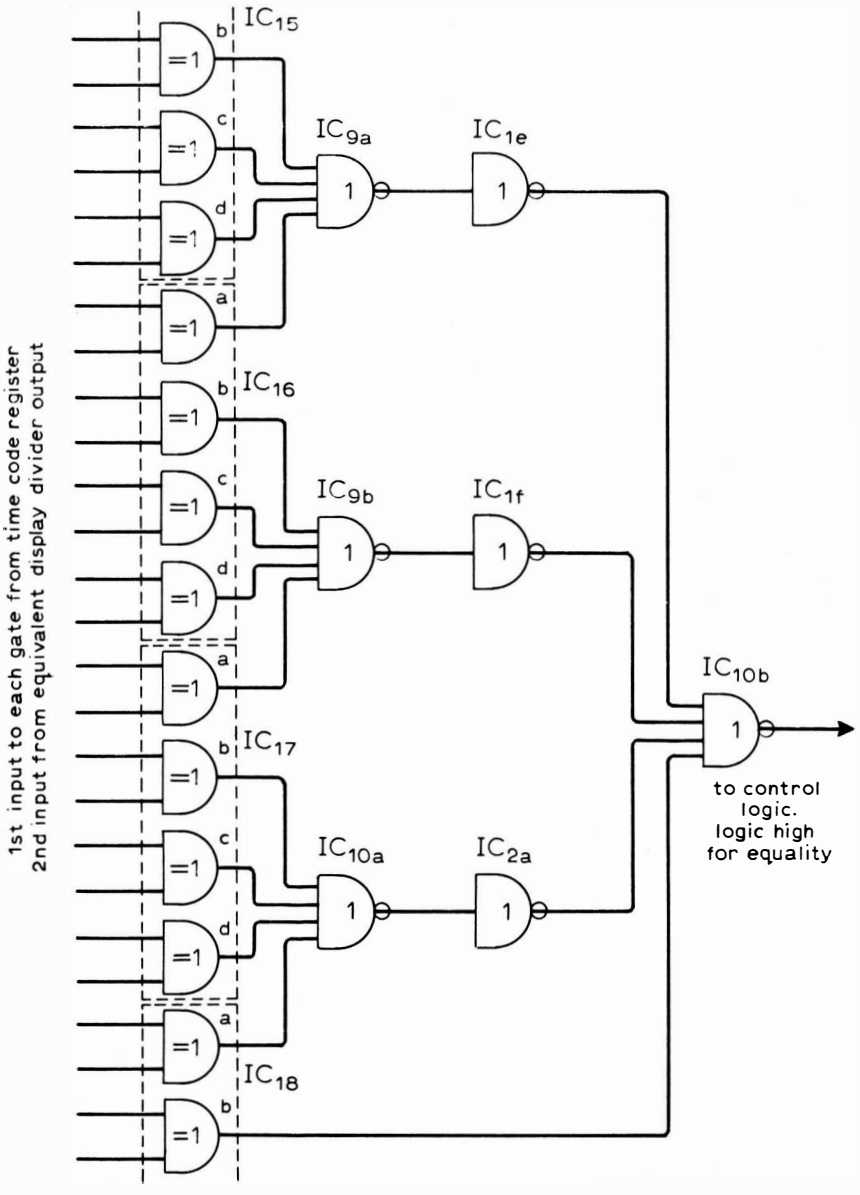
Fig. 8. Timing diagram for control pulse detection.

which the muting circuit operates. In areas of high signal strength, the muting circuit can operate at a higher signal level, thereby improving the interference rejection when the carrier is not present. With a weaker signal, the muting circuit must be set to operate at a lower level. Transistor Tr_6 is the demodulator and, with no signal present, is biased off. With a carrier signal, the positive peaks turn Tr_6 on which discharges C_{17}. The potential on C_{17} is detected by Tr_7 which, with Tr_8, produces a 5V demodulated signal. Resistor R_{20} provides a small measure of positive feedback to assist clean switching. The output from Tr_8 is fed to the time-code-register logic, and also drives a l.e.d. indicator (carrier).

The time-code-register, Fig. 7, takes in the demodulated signal, detects the control pulse and stores the incoming time code. It also checks the parity of the detached signal and generates a data-strobe pulse when the register is full. Transistor Tr_9 produces a 5μs pulse for every carrier-off transition. This pulse is used to trigger monostable IC_{32a} (23ms), whose trailing edge triggers monostable IC_{32b} (20mS). The differentiated trailing edge of the second monostable pulses the transistor Tr_{10} which delivers an output of about 4ms. The output of gate IC_{8a} inhibits retriggering of the monostable chain during its active period, i.e. for 47ms. Gate IC_{8a} also applies a reset level to the cross-coupled NAND-gate bistable IC_{2b}/IC_{3a}, which is removed for the 47ms period. The timing of the internally generated pulses in relation to the demodulator output is shown in Fig. 8. The action of the detector is best explained if monostable IC_{32a} is imagined to have a period of 25ms, and monostable IC_{32b} a period of 18ms; the reason for modifying these periods will be explained later.

The detector attempts to mimic the expected incoming waveform of the control pulse. The Q output of the first monostable, once it has been triggered,

Fig. 9. Comparator circuit which compares 13 inputs from the time-code register with the hours and minute-divider output.



goes high for 25ms, and then low. This is exactly the signal out of the demodulator when a control pulse is received. The two signals are compared and any difference results in the output of exclusive -OR gate IC_{15a} going high, and the cross-coupled NAND-gate bistable becoming set (output of IC_{2d} low). Because it is impossible to mimic exactly the 25ms off-period, a degree of tolerance is allowed by shortening the monostable period to 23ms and producing at the end of the period, a 4ms inhibit pulse (Tr_{11}, Tr_{12}) which prevents the setting of the bistable around the time of the carrier-on transition. The timing allows a total error of up to 2ms either way. The 4ms pulse from Tr_{10} generates a gating window for the period 43ms to 47ms after the initial triggering of the 23ms monostable. Its output is applied to the 3-input NAND gate (IC_{8b}). For a low pulse on the output of the gate, three input conditions must apply; the 4ms window must be open, the bistable must not have been set, and an off-transition pulse must appear on the collector of Tr_9. The low output pulse represents the end of the control pulse.

To summarise; after receipt of an off-transition, a continuous high for 23ms is sought, followed by a continuous low from 27ms to 43ms, again followed by an off-transition between 43ms and 47ms. The signal will be ignored if there is any deviation from these conditions. This detection technique has been found to give extremely good immunity against false triggering due to noise. The low pulse generated on the output of IC_{8b} resets the two 8-bit serial-in shift registers ($IC_{38\ \&\ 39}$). All outputs go low. When pin 13 of the second register goes low it removes the reset-to-nine signal from the clock generator IC_{20} which is a divide-by-10, clocked by a continuous 1kHz signal from the 5-decade divider chain. Upon removal of the reset, it starts to generate a 100Hz signal on its D output, the first positive transition occurring between 8ms and 9ms after the removal of the reset, and thereafter at 10ms intervals. This signal is applied to the clock input of the shift registers, thereby clocking in the time code applied to the input of the first register.

The first data bit in the time code is always a 1; after 16 clock pulses this 1 will have reached the last bistable in the second shift register (pin 13). This output restores the reset to the clock generator which stops the clock pulses. The register now contains the complete time code, including leading marker bit and parity bit. The parity is checked by using a JK flip-flop (IC_{12a}) to count the number of 1's appearing at the first shift register output as the data is clocked through. For every 1 clocked into the register, the J and K inputs become logic 1; when clocked, the JK flip-flop inverts its previous state. For a 0 on the J and K inputs, the output state does not change when the flip-flop is clocked. Thus the final state of the JK flip-flop is determined by whether an even or odd number of 1's have been clocked into the register. The flip-flop starts in the reset state, Q = 0; if received parity is correct the final state is Q = 1. Gate IC_{8c} generates the data-strobe pulse of 2μs about 200ns after the full signal is received from the shift register, and in the presence of correct parity. The data-strobe pulse is passed to the control logic. The data-clock enabling signal is used to drive the code indicator D_5, which will light for about 150ms upon recognition of a control pulse.

Thirteen inputs from the time-code register are compared with the hours and minutes divider outputs — Fig. 9. Thirteen exclusive -OR gates ($IC_{15,\ 16\ \&\ 17}$) each compare one bit, giving a logic 0 output for input identity and a 1 for disparity. The first twelve outputs are OR-ed via inverted NOR gates, and these outputs are again OR-ed, along with the thirteenth bit comparison, by NOR gate IC_{10b}, producing a logic high for no comparison error.

(To be continued)

Sixty Years Ago

The principle of redundancy, or the "belt and braces" approach to the achievement of reliability, is common enough, but for those who imagined it to be a modern, money-no-object attitude, the following piece from our issue of February, 1915, is some indication to the contrary. It rather reminds one of the writers who advocate the use of electronic ignition devices, but recommend the use of a changeover switch for instant reversion to the mechanical system.

"Every means of long-distance communication has been used in this war, and although the carrier pigeons' loft in the South of England, long utilised by the British Admiralty, was dismantled a few years ago on account of the introduction of wireless telegraphy, we know that pigeons are still being used by the British for war purposes. Only quite recently the War Office authorities issued instructions to the effect that it was hoped that British sportsmen who were not able to distinguish between ordinary wood pigeons and carrier pigeons would abstain from pigeon shooting altogether. The reason for this appears to have been that some of our own sportsmen were destroying British flying dispatch bearers. The fact of the matter with regard to all these things is that the latest method may for all ordinary purposes supersede its predecessors; but in times of strain and stress it is wise to have as many strings to one's bow as possible."

Literature Received

Magnifiers for desk use, quality control and inspection, including the illuminated variety, spectacle types and eye magnifiers are described in an illustrated brochure from Combined Optical Industries Ltd, 200 Bath Road, Slough, SL1 4DW WW407

A seven-volume collection of data on Motorola semiconductor devices is now available. Devices from other manufacturers are covered in broad outline. Four of the books, the index and three volumes of discrete devices, are available at £10.50, while those concerned with emitter-coupled logic, complementary m.o.s. and linear i.cs are priced at £6. The complete set costs £15. Motorola Ltd, Semiconductor Division, York House, Empire Way, Wembley, Middlesex HA9 0PR.

Plessey have produced an illustrated brochure on its range of resistors of various kinds, including faders, cermet power resistors, potentiometers and trimmers. R.f. chokes are included. Plessey Resistors, Cheney Manor, Swindon, Wilts SN2 2PZ WW408

A complete catalogue of the prolific Foulsham range of books on hobbies and technical subjects, including electronics, is obtainable from Foulsham-Tab Ltd, Yeovil Road, Slough SL1 4JH WW409

A comprehensive listing of all known professional resistors in Western Europe has been compiled by the European Space Agency as an introductory volume in a series covering all components. The lists will be published annually. The Resistance Reference Book is obtainable free from ESRIN/SDS, Electronic Components Databank, Casella Postale 64, 1-00044 Frascati (Roma) WW410

Aerialite have sent us the first two leaflets in their new series, which describe and illustrate u.h.f. aerials and a range of coax. plugs and sockets, diplexers and a masthead amplifier. Aerialite Aerials Ltd, Whitegate, Broadway, Chadderton, Oldham, Lancs OL9 9QG WW411

A shortform catalogue is obtainable from AMI Microsystems, which lists current and future projects in the field of microprocessors, memories, communication modules, watch and clock circuits, calculator chips and displays. AMI Microsystems Ltd. 108A Commercial Road, Swindon, Wilts WW412

We have received a data sheet from ITT, which gives constructional and application details on their transformers and coils. It can be obtained from ITT Components Group Europe, Electrical Products Division, Edinburgh Way, Harlow, Essex WW413

British Standard BS 1597 "Radio interference suppression on marine installations" is now revised. Copies are available at £3.50 from BSI Sales Department, 101 Pentonville Road, London N19ND.

A brochure is available on the ELLM earth line and leakage monitor which prevents the connexion of a piece of equipment to the mains via a circuit breaker if a leakage of over 30mA exists or if a sufficiently good earth is not provided. Commercial and Industrial Electrical Services Ltd, 73-75 Shawhill Road, Birmingham B8 3LJ WW414

Correction

In the November issue we stated that Custom Transformers offered only the mechanical components for transformers. This was wrong — a winding service is provided. We apologize for the error. The catalogue is obtainable from Custom Transformers Ltd, Bristol Road, Malmesbury, Wilts SN16 0DU, and covers units from 5 to 1500VA WW415

Time-code receiver clock — 2

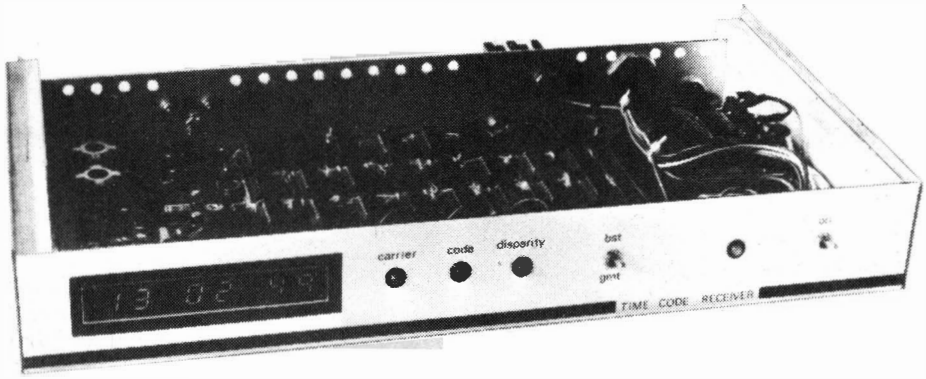
Control logic and display

by A. F. Cross, B.Sc.

Thames Television Ltd

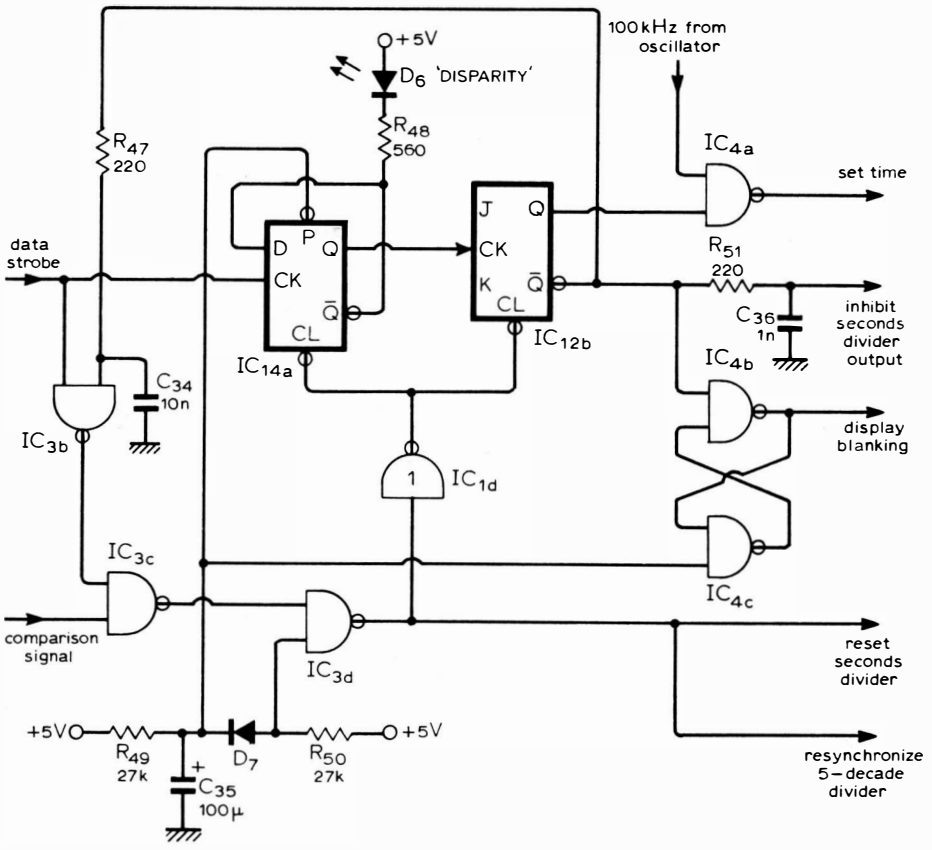
The control logic is shown in Fig. 10. A negative data-strobe pulse from the time-code register is applied to the clock input of the D-type flip-flop IC_{14a}. This operates as a divide-by-2, and is clocked by the data-strobe pulse. If, at the time of the data-strobe pulse, the comparator logic indicates no disparity between the incoming data and the display-dividers, a simultaneous reset pulse is applied to the clear input of the D-type via gates $IC_{3b,c,d}$ and inverter IC_{1d}. Thus the clock pulse will have no effect. If, however, the comparator is indicating disparity, the reset will not be applied, and the data strobe will clock the D-type into the 1 state. This is remembering that a disparity has arisen, but no action is taken apart from lighting the disparity indicator (the benefit of the doubt is given to the display-dividers). One of two things can happen on the next code one minute later; if no disparity is signalled by the comparator the D-type will be reset, and the previous disparity ignored. If a second disparity is indicated the reset pulse will not appear, and the clock pulse will now cause the D-type to revert to the 0 state, clocking the JK flip-flop IC_{12b} to a 1 as it does so. With the JK flip-flop's Q output at 1, gate IC_{4a} is enabled and passes 100kHz pulses into the minutes and hours-dividers, thus advancing the indicated time. When the time in the hours and minutes-dividers becomes equal to the received code, the comparator produces an equal signal which resets the JK and D-type flip-flops, thus disabling the 100kHz clock pulses. The inhibit-seconds-output signal from the Q output of the JK flip-flop ensures that gate IC_{4d} in Fig. 3. does not inhibit the 100kHz pulse train. The data-strobe signal also resets the seconds dividers and resynchronizes the 5-decade divider, so long as there is no comparator error signal.

The initial conditions upon switching on the clock are provided by C_{35}, D_7 and the cross-coupled NAND-gate ($IC_{4b,c}$) bistable. Capacitor C_{35} is initially discharged and presents a 0 to the input of IC_{3d} via diode D_7. Thus a low reset is provided on the clear inputs to bistables a and b via inverter IC_{1d}. However, the



Complete clock showing one matrix board containing all the circuitry except for the power supply.

Fig. 10. Control logic.



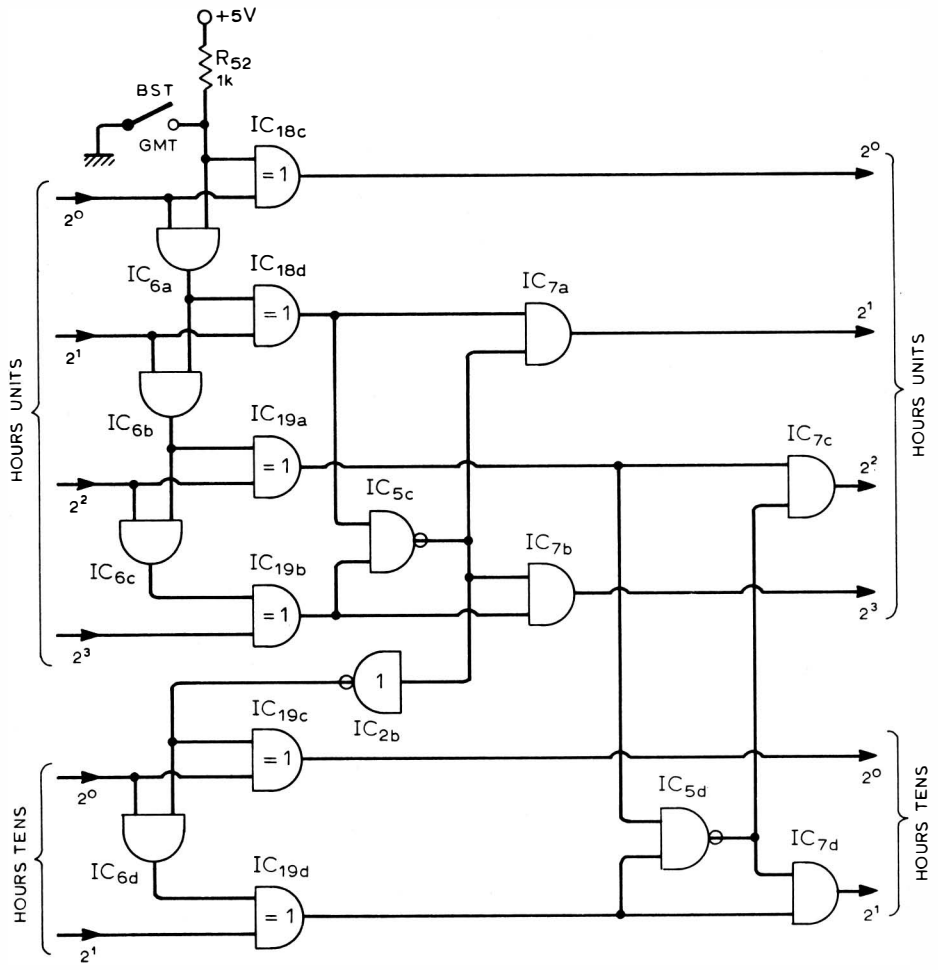


Fig. 11. GMT/BST converter. This section adds one to the hours code presented to its input, and is essentially a simplified binary adder.

preset condition is also applied to bistable a. As C_{35} charges its potential rises and diode D_7 ensures that the logic 0 disappears from the input of IC_{3d} (and therefore from the clear inputs of the bistables) before the preset is removed from bistable a. This bistable is left in the set state, and bistable b in the reset state. The disparity lamp will light, and on the first received time code the display dividers will be set to match it, rather than the normal running procedure of waiting for the second received code before setting the display dividers. The cross-coupled NAND-gate bistable is also reset by capacitor C_{35}, and set when the $\bar{Q}$ output of bistable b goes low, which occurs when the control logic is setting the time in the display-dividers. The output of IC_{4b} controls the blanking input to the b.c.d.-to-7segment decoder-driver. Thus, on switching on, the display will be blanked until the first time code is received.

The GMT/BST Converter, when enabled, adds one to the hours code presented to its input as shown in Fig.

Component list

Resistors (all ⅓W, 5% unless stated)

R1, 2, 3	220k	31	220
4	10k	32	56k
5, 6	220k	33	4k7
7	10k	34	10k
8	33k	35	4k7
9	18k	36-39	220
10	3k9	40	560
11	2k2	41	470k
12	1k5	42	2k2
13	4k7	43	470k
14	1M	44	10k
15	82k	45	4k7
16	4k7	46	330
17	470k	47	220
18	100k	48	560
19	27k	49, 50	27k
20	3M3	51	220
21	270	52	1k
22	330	53-58	4k7
23	10k	59-64	820
24	1k	65-71	270
25	4k7	72	180, ½W
26	15k	73	20k skelton preset
27	10k	74, 75	10k skeleton preset
28	15k		
29	2k2		
30	4k7		

Capacitors (± 10% unless stated)

C1	1n polystyrene
2	500p Trimmer (RS Components)
3, 4, 5	100n
6, 7	5n polystyrene (4n7 + 270p) see text
8-14	100n
15	2μ2 10V electrolytic
16	47μ 10V electrolytic
17	33n
18	1n
19, 20	4μ7 35V tantalum bead (± 20%)
21	470n
22	100n
23	1n
24, 25	10n
26	1n
27	10n
28	4-20p trimmer
29	39p silvered mica (RS Components)
30	500p silvered mica (RS Components)
31	1n5 silvered mica (RS Components)
32	33p
33	2μ2 10V electrolytic
34	10n
35	100μ 10V electrolytic
36	1n
37	4,700μ 16V electrolytic
38	10μ 10V tantalum bead

Additionally a 10n ceramic disc across the 5V supply at each i.c. is recommended.

Integrated circuits

IC	Function	Type No
1	Inverter	SN7404N
2, 3, 4, 5	2-I/P NAND	SN7400N
6, 7	2-I/P AND	SN7408N
8	3-I/P NAND	SN7410N
9, 10	4-I/P NOR	SN7425N
11	B.c.d./7 segment decoder	SN7447AN
12, 13	J-K flip flop	SN7473N
14	D-type flip flop	SN7474N
15, 16, 17, 18, 19, 20, 21, 22, 23, 24	Exclusive -OR	SN7486N
25, 26, 27, 28	Decade counter	SN7490N
29, 30, 31	Divide-by-12	SN7492N
32	Monostable	SN74123N
33	One-of-ten decoder	SN74145N
34, 35, 36, 37	8-I/P Multiplexer	SN74151N
38, 39	8-bit shift register	SN74164N
40	5-volt regulator	LM309K

Transistors

Tr 1-8	BC 108
9-12	2N4123
13, 14	BC 108
15	2N4123
16-21	MPS6534 (Motorola)

Diodes

D1, 3, 4	1N 914
2	Light emitting diode: yellow (RS Components)
5, 6	Light emitting diode: red (RS Components)
7	OA47
8	Full wave bridge, type REC 76 (RS Components)
9	Light emitting diode: green (RS Components)

Display
Seven segment l.e.d. type, Litronix DL 707 (Forward drop 1.7V at 20mA): 6 required

Crystal
100kHz type MG5X (Quartz Crystal Co. Ltd)

Transformers

T1, 2	Wound on Mullard Cores type LA 1416 (adjuster LA 1503): Primary: 100 turns 36 s.w.g. (1.42mH) Secondary: 10 turns 36 s.w.g.
3	Mains transformer 20VA. 9V r.m.s. (RS Components, type 207-122)

Aerial
Ferrite rod 8in × 5/16in diameter, Denco.

Miscellaneous
Heatsink for regulator 8°c/W or better. Mains fuse 300mA slow.

11. It is essentially a simplified binary adder, with modifications to cater for the decimal count and twenty-four hour reset. The BST enable signal is effectively a one-bit number which is added to the six-bit hours code. With the BST enable line at logic 1 (switch open), a 1 is added to the GMT code to produce a BST output; with the BST enable line at logic 0, nothing is added to the incoming hours code and it passes unaltered through the converter. Gates IC_{6a} to IC_{6d}, $IC_{18d,\ d}$ and $IC_{19a,\ b,\ c,\ d}$ perform the add function. The operation on each bit is identical. The first addition is performed by exclusive —OR gate IC_{18c} and the AND gate IC_{6a}. With the switch closed, a 0 is presented to one input of each gate; thus the AND gate is inhibited, and the output of the exclusive —OR gate follows the hours code input. With the switch open, a 1 is applied to one input of both gates. When the hours code 2^0 input is a 0 the BST bit will convert the output of the exclusive —OR gate to a 1, but, because the code input is low, it inhibits the AND gate; no carry is therefore passed to the next stage. With the hours code 2^0 input at logic 1, the gates provide the required 0 output on the 2^0 line and a carry bit to the next significant level where the process is repeated on the 2 input. Because speed is unimportant, this ripple-through technique is quite suitable.

Truth table for multiplex clock

Output code of + 12

D	C	B	A	Digit enabled
X	0	0	0	Tens of hours
X	0	0	1	Units of hours
X	0	1	0	Tens of minutes
X	0	1	1	Units of minutes
X	1	0	0	Tens of seconds
X	1	0	1	Units of seconds
X	0	0	0	Tens of hours
X	0	0	1	Units of hours
	etc			etc

(X = irrelevant)

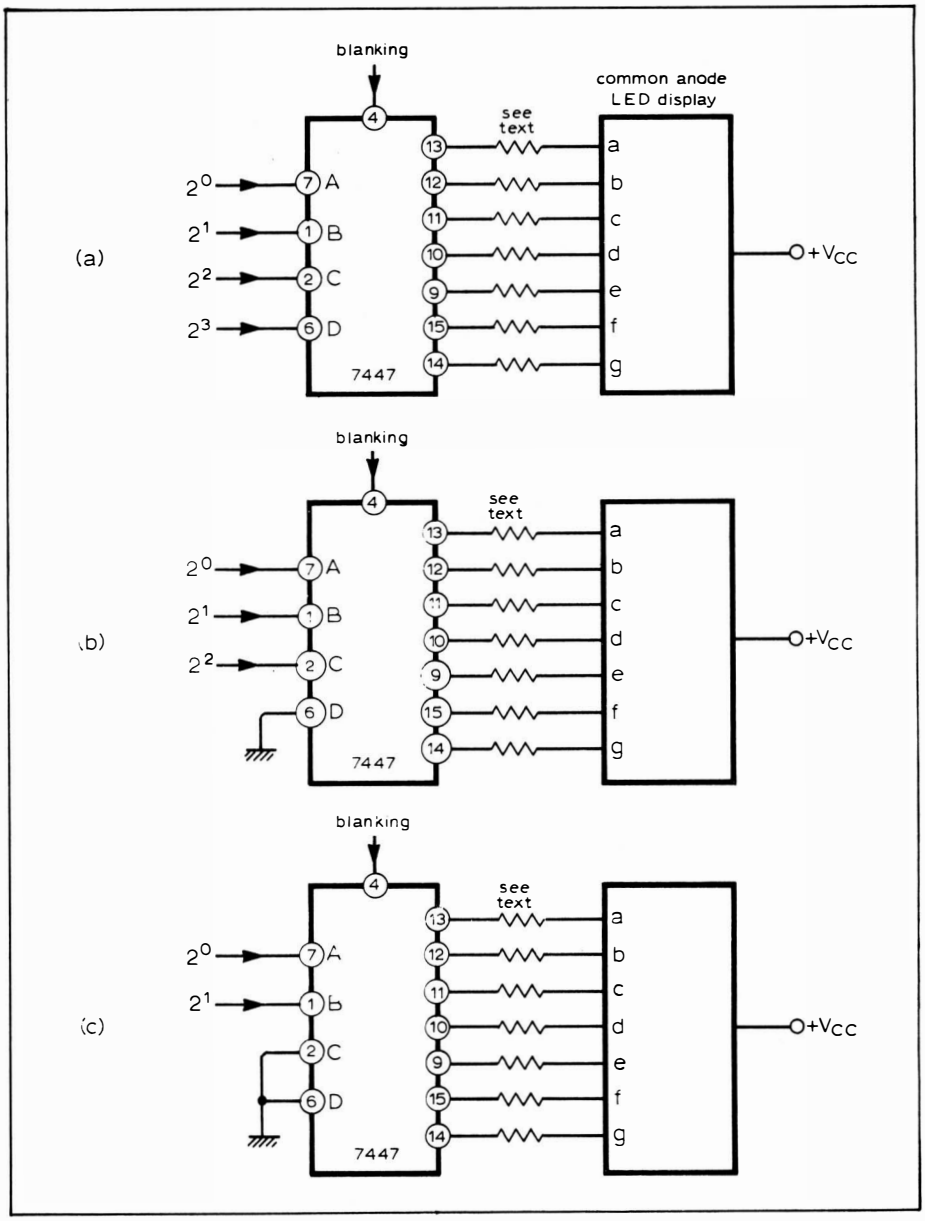


Fig. 12. (a) Drive for units of hours, minutes and seconds (3 required), (b) drive for tens of minutes and seconds (2 required), and (c) drive for tens of hours.

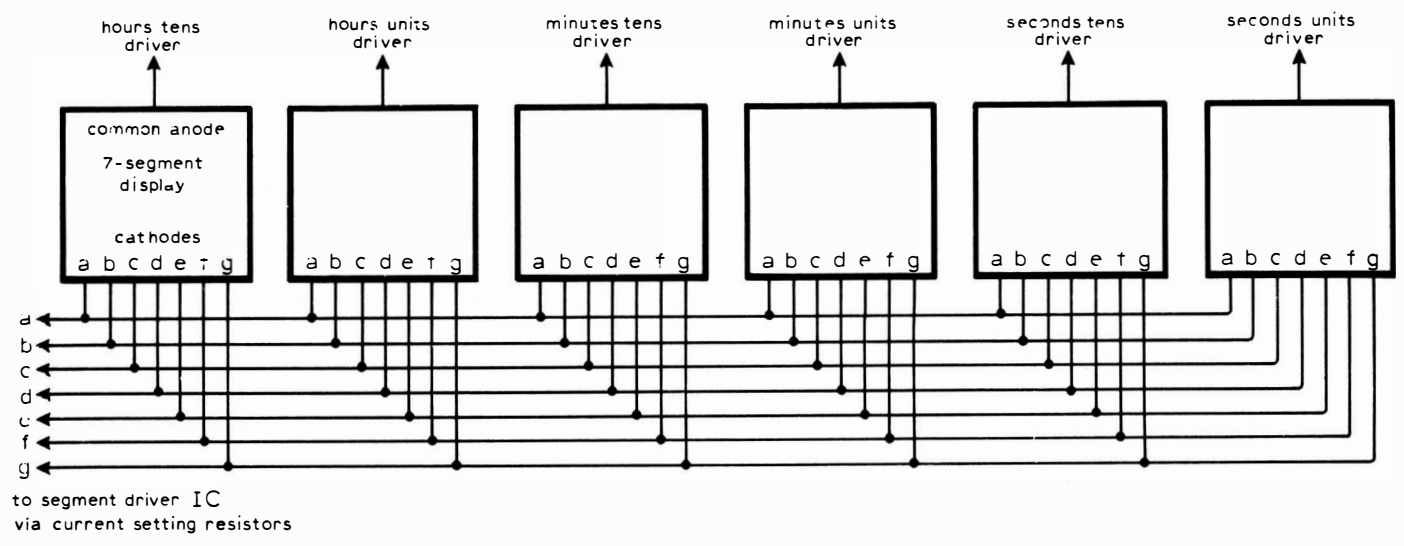


Fig. 13. Multiplex connection details for display which uses a total of six anode and seven cathode connections.

Gate IC_{5c} detects the condition 1010 (decimal value 10) on the hours-units output, produced by a decimal value 9 input. When this happens the hours units must have an output 0000 and a carry must be passed to the tens-of-hours. A low output from IC_{5c} inhibits the outputs of gates IC_{7a} and IC_{7b}, which produces the carry 1 from inverter IC_{2b} for the tens-of-hours adder. Gate IC_{5d} detects the decimal value 24 (10 0100) on the output of the adder and inhibits the gates IC_{7c} and IC_{7d} to produce the required all-zeros output.

Display

The display can take several forms, using either numerical indicator tubes or seven-segment displays. The author's clock uses seven-segment l.e.d. displays. Two modes of display operation have been used by the author and both are described.

The simplest method uses a SN 7447 AN b.c.d.-to-seven-segment decoder-driver for each digit, as shown in Fig. 12. Any unused data inputs to the decoder must be grounded. The resistors between the decoder outputs and the segment cathodes set the currents to about 10mA. Supply potentials other than 5V may be used for the display, provided that the resistor value is adjusted and the voltage rating of the decoder output is not exceeded. It may be convenient, for example, to run the display from the d.c. supply feeding the 5V regulator, rather than from its output, to reduce the current demand on the regulator. This parallel method of driving the displays, while simple in principle, does involve 42 current-setting resistors, and 43 connections to the display board. For about the same component cost, but with only seven current-setting resistors and thirteen display board connections, the multiplex mode of operation may be used. This has been adopted for the prototype clock and is shown in Fig. 14.

With this method the digits are not driven simultaneously, but in sequence, and at a rate which appears as a continuous drive of all digits. Only one b.c.d.-to-seven-segment decoder-driver is used, which receives in turn the input code for each digit. In this case each digit code is applied for 1mS, and is repeated every 6mS. Synchronously, with each digit code being applied to the decoder-driver input, the appropriate common anode connection is switched to the supply rail by the associated driver transistor. The multiplexing of the six-digit codes into the decoder-driver is performed by four 8-input multiplexers, type SN 74151N. The digit code is selected by the three-bit code applied to the selector inputs of the multiplexers, and derived from the A, B and C outputs of the divide-by-12, IC_{31}. The counting sequence, and the digit-code enabled for each state are shown in the table. The count outputs are also applied to the inputs of the 1-of-10 decoder, IC_{33}. Each input state produces one low output only, and this is used to switch on the anode driving transistor for the display digit whose code is currently controlling the display cathodes. Because only one digit common-anode is driven at any time, the equivalent cathodes in all displays may be connected together as shown in Fig. 13. This results in a total of six anode and seven cathode connections.

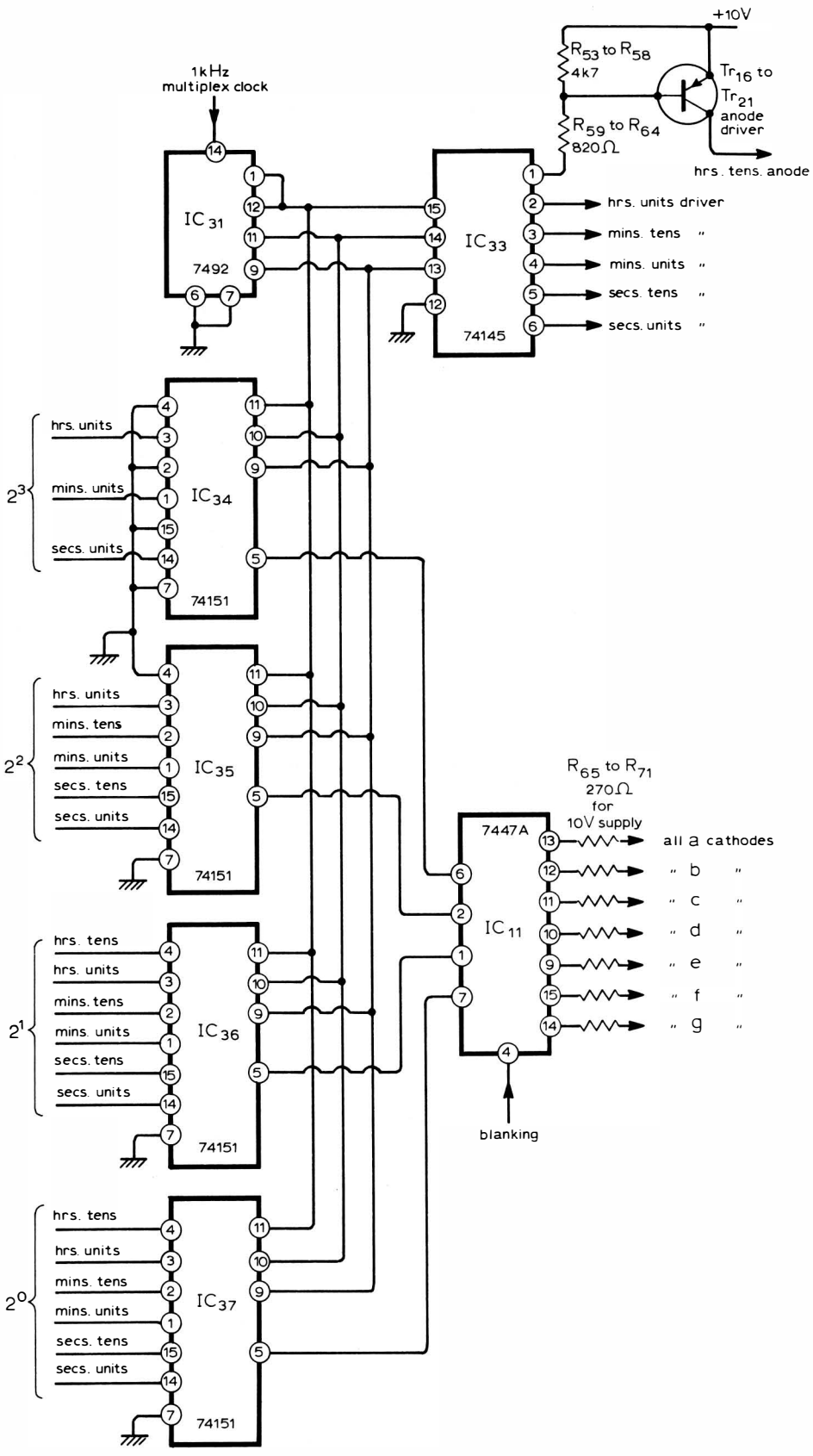


Fig. 14 Multiplex display logic drivers. This method of driving the displays only requires seven current-setting resistors and thirteen display board connections.

Time-code receiver clock — 3

Construction, alignment and operation

by A. F. Cross, B.Sc.

Thames Television Ltd

The power supply for the time-code receiver clock, shown in Fig. 15, requires little explanation. The nominal d.c. voltage across C_{37} is 10V on load, and this can be used to supply the display. The 10V rail feeds the monolithic voltage regulator IC_{40}, which has an output preset to 5V, and a current output capability in excess of 1A. A heat-sink is required for the regulator.

Construction

The author's aim was a conveniently small clock, and for this reason a compact layout has been adopted. Apart from the power supply, the clock has been constructed on one matrix board 10in × 6in, resulting in overall dimensions of 14in × 7in × 2½in.

Care should be taken with the layout, and the power supply connections should be as short and substantial as practical e.g. at least 20 s.w.g. on the board. It is good practice to decouple the supply rail to the integrated circuits at regular intervals; a 10nF ceramic disc per integrated circuit is ideal. Logic wiring should be no longer than necessary, and compact construction of the receiver will minimise the effect of interference from the logic. Earthing of the zero-volt line is important, preferably to a single point on the chassis. For this reason it is desirable to isolate the aerial coaxial socket, the 5V regulator can then become the common earth point.

The displays are mounted in d.i.l. sockets fitted to a small piece of matrix board, and interconnected using thin single strand insulated wire. The wiring details of the ferrite-rod aerial are shown in Fig. 16. The rod may be housed in a plastic or cardboard tube, along with the tuning capacitors which should have short connections to the coil. A screened cable should be connected as shown, close to the coupling coil. The siting of the aerial should not be critical except in areas of low signal strength; however, placing it within six inches or so of the clock does result in a degradation of the signal due to interference from the power supply. Generally it is more convenient to separate the aerial from the clock so that it may be independently rotated for the best signal. The capacitors across the primary windings are a parallel combination of a nominal 4n7 capacitor plus a smaller value for trimming. The final adjustment of resonant frequency is made with the coil adjuster core.

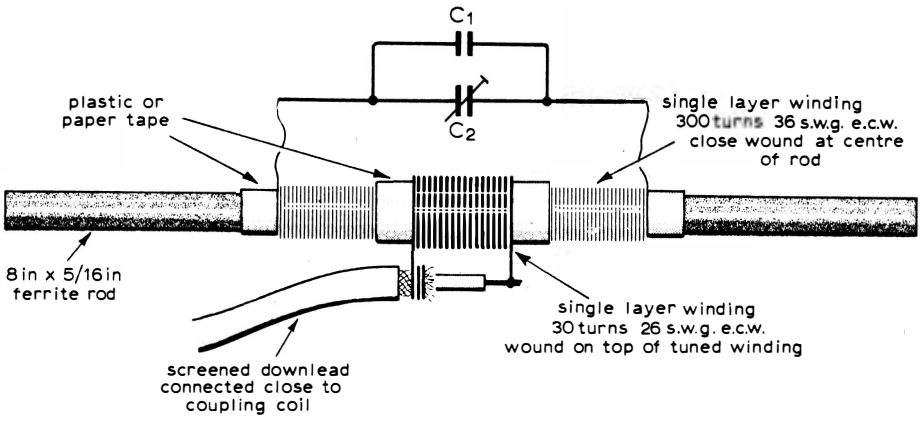


Fig. 16. Ferrite-rod aerial constructional details.

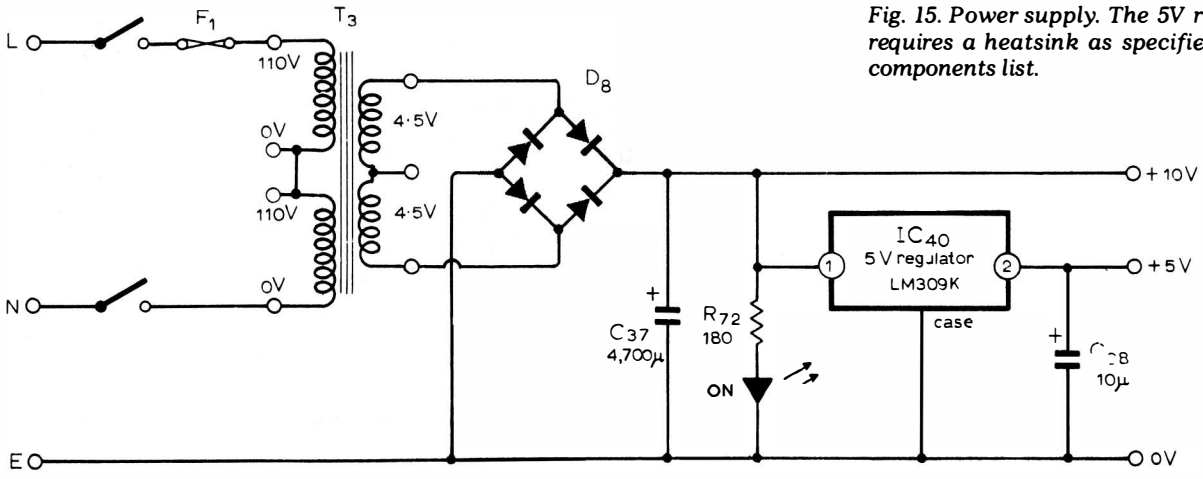


Fig. 15. Power supply. The 5V regulator requires a heatsink as specified in the components list.

Alignment

There are several adjustments to be made before the clock will function correctly. These are; tuning of the ferrite-rod aerial, alignment of the two tuned amplifier stages, adjustment of the muting level, adjustment of the crystal oscillator frequency, and the setting of the two monostable periods.

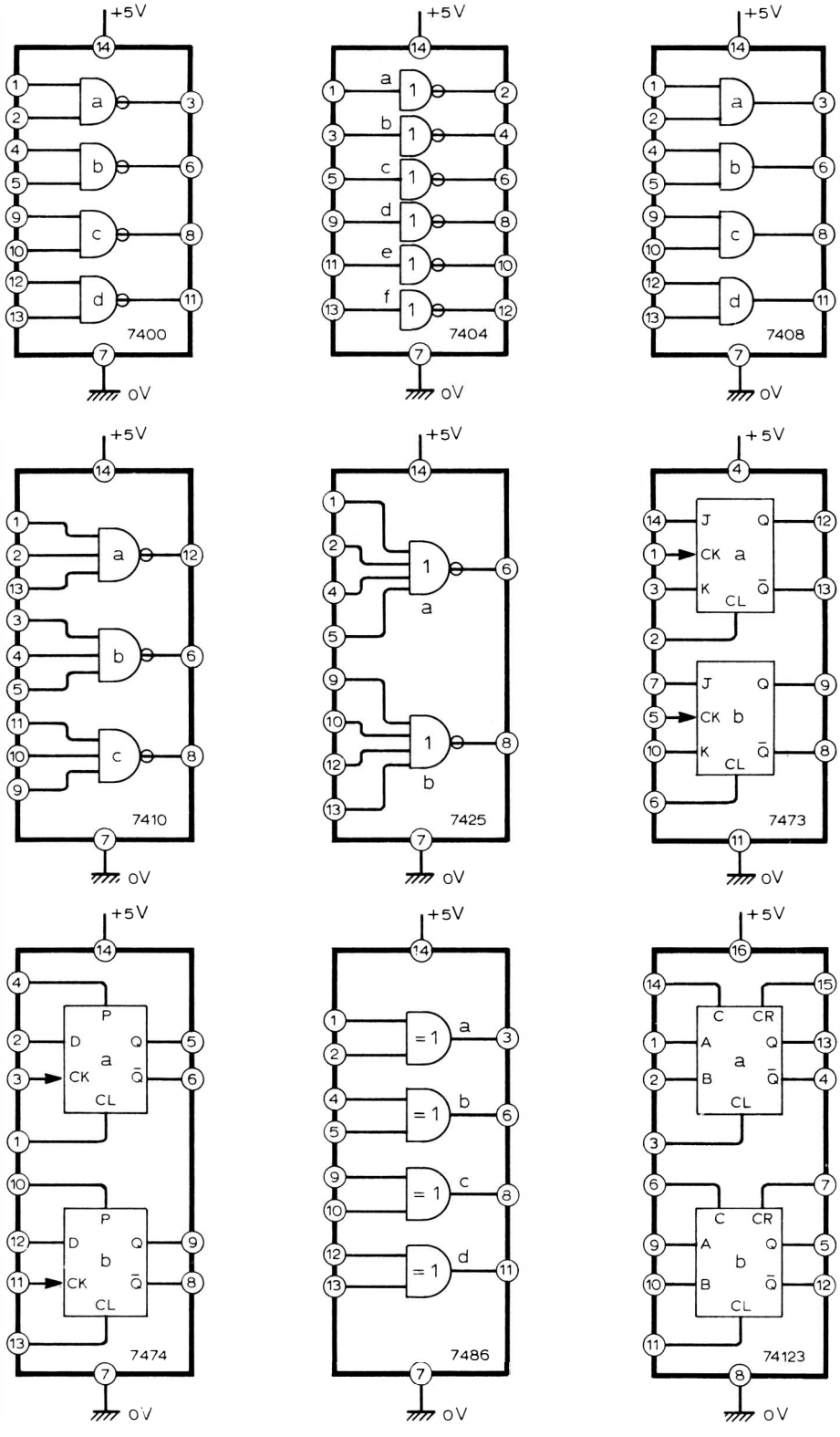
The a.g.c. used in the receiver must be disabled before accurate alignment is possible. For the initial tuning, however, there will probably be insufficient output to operate the a.g.c. system and the amplifier will be operating at maximum gain. An oscilloscope should be connected to the collector of Tr_3. The adjusters for T_1 and T_2 should be set about half way. With the ferrite rod placed roughly "broadside" to Rugby, the aerial trimmer C_2 should be adjusted over its range until a 60kHz signal is observed on the oscilloscope (this may be only a few millivolts). T_1 and T_2 are now adjusted for maximum output. When the output has reached about 600mV peak-to-peak, the a.g.c. loop will start to operate. To disable this a 47kΩ potentiometer should be connected between the collector of Tr_4 and zero volts. This is now adjusted to give an output between 100 and 200mV peak-to-peak. Fine adjustments to all three tuned circuits can now be made, adjusting the potentiometer as necessary to maintain the output below 200mV. When tuning is complete the potentiometer is removed; the output should increase to between 600mV and 800mV peak-to-peak. (The positive peaks will be somewhat flattened due to non-linear loading of the output.)

Muting level is set by adjusting R_{73}. (With the receiver correctly aligned, the carrier indicator lamp should be flashing with the breaks in the carrier.) When R_{73} is set to maximum resistance the muting level is at a minimum, i.e. relatively weak signals can be received without the muting circuit inhibiting the demodulator. This means, however, that in areas prone to radio interference, such interference may be of a level which prevents the muting circuit from operating when Rugby is not transmitting. If the normal signal strength is good, the muting level can be raised to reject the interference.

The oscillator is easily set to the correct operating frequency, using the received 60kHz carrier as a reference. The output of the first decade divider after the oscillator (pin 11, IC_{21}) provides a 10kHz signal; this is used to trigger an oscilloscope with the timebase set at about 5μs/cm. Displaying the signal on the collector of Tr_3 in the receiver should produce a stable 60kHz trace which drifts slowly across the screen. The trimmer, C_{28}, is now adjusted for minimum drift. Because one cycle of the 60kHz carrier has a period of 16.7μs, a figure for the accuracy can be determined. A relative drift of one cycle per second represents 16.7μs per second or 16.7 parts per million. Ideally the oscillator should be set up to better than one part per million which requires that the relative drift be one cycle of carrier in not less than about 17 seconds (the breaks in the displayed carrier provide convenient one second pulses for timing).

The adjustable monostable periods can be set up using an oscilloscope with a well-calibrated time base (an excellent calibrator is the crystal oscillator and divider chain). The demodulated carrier will normally trigger the monostables once per second. The final adjustment should be made by comparison with the received control pulse once per minute. The end of the 25ms off period (preceding the control pulse) should fall in the middle of the 4ms low pulse on the collector of Tr_{12}; R_{74} is adjusted to achieve this. The end of the 20ms control pulse should fall in the middle of the 4ms high pulse on the collector of Tr_{10}; only R_{75} should be adjusted for this.

Fig. 17. Connection details for integrated circuits.



Operating the clock

When the clock is switched on the disparity lamp should light, along with the carrier lamp which flashes in sympathy with the signal. Besides the one-second pulses, the time code should be seen as a brief flicker each minute. The other coded information may also be noticed: firstly, the atomic/astronomic time-difference code, which is transmitted as a double break in the carrier in some of the seconds in the first quarter of each minute. This code changes from week to week as the difference varies. Secondly, in the last five seconds of every hour, the modulation is changed to the station call sign (MSF) transmitted twice in Morse code. Until the first code is correctly received, the clock display remains blanked. Upon recognising a control pulse the code lamp should flash, the disparity lamp should go off, and the display should show the received time code (subject to the GMT/BST switch). The disparity light may come on again if either a spurious signal is recognised as a control pulse (followed by correct spurious parity), or if the time code is incorrectly received (but again with the correct detected parity), or if the contents of the display dividers become corrupted by, for instance, momentary loss of power. For the displayed time to become corrupted by received interference, several coincidences must occur; two false control pulses need to be recognised with no intervening correct code, also, both false pulses must be followed by correct parity before they are acknowledged by the control logic. Although the chance of this happening is increased when the transmitter is switched off, the system has been found to give satisfactory results in most environments.

The author wishes to thank Mr J S Sansom, OBE, former director of Studios and Engineering, Thames Television, for permission to publish this article, and Mr B G Scott, chief engineer, for his encouragement and the use of facilities for the project.

Points arising

Because of a change in the transmission specification the following points should be noted. In Fig. 1 the parity bit was shown as a 1, this is now a 0 and, as a result, the parity check from IC_{12a} (Fig. 7) is taken from the $\overline{Q}$ output. If the received parity in the flip-flop is correct the final state is now $Q = 0$.

In the parts list IC_2 was shown as a quad two-input NAND gate package. In Fig. 9, 11 sections a and b of IC_2 are shown as inverters. These are realised by connecting the two inputs of the gates together which then function as inverters.

Meetings

LONDON

1st. IEE — "Electrical engineering and medicine" by Dr D. W. Hill at 18.30 at Savoy Pl., WC2.

6th. IEE — "Position control of floating structures" by P. H. Barton at 17.30 at Savoy Pl., WC2.

7th. IEE — "The history of transmitters — some aspects of early radio" by R. F. Pocock at 17.30 at Savoy Pl., WC2.

7th. BKSTS — "What are audio visuals?" at 19.30 at Thames Television Theatre, 308-316 Euston Road, NW1.

12th. IEE — "Digital systems representation" by S. Y. Foo at 18.30 at Savoy Pl., WC2.

13th. IEE — Colloquium on "Earth leakage protective devices" at 10.30 at Savoy Pl., WC2.

13th. IEE — Colloquium on "Theory and operation of Read type IMPATTs" at 14.30 at Savoy Pl., WC2.

13th. AES — "Developments in noise reduction techniques" by speaker from Dolby Laboratories Inc. at 19.15 at the IEE, Savoy Place, WC2.

14th. IEE — Colloquium on "Evaluation and experience of high level languages for process control computers" at 10.30 at Savoy Pl., WC2.

20th. SERT — One-day seminar on "Applications of computers" at the IEE, Savoy Pl., WC2.

21st. IERE — Colloquium on "Automatic production" at 14.00.

21st. BKSTS — "Video tape recording today and tomorrow" by L. H. Griffiths at 19.30 at Thames Television Theatre, 308-316 Euston Road, NW1.

26th. IEE — "History of magnetic sound recording" by B. Lane at 17.30 at Savoy Pl., WC2.

27th. IEE — Colloquium on "Paging systems" at Savoy Pl., WC2.

29th. IEE — Colloquium on "Parallel digital computing methods: d.d.as and stochastic computing at 10.30 at Savoy Pl., WC2.

29th. IERE — "A novel approach to marine surveying" by J. M. Thompson at 9 Bedford Sq., WC1.

30th. IEE — Discussion on "Part-time undergraduate degree courses in electrical engineering" at 17.30 at Savoy Pl., WC2.

BELFAST

13th. IEE — "Integrated circuits for communications" by S. J. Laverty at 18.30 at Ashby Institute.

BIRMINGHAM

7th. IEE — "Train control, developments on British Rail" by J. W. Birkby at 18.30 at Sumpner Building, University of Aston, Gosta Green.

14th. RTS — "The other side of the camera" by Tom Coyne at 19.00 at BBC Broadcasting Centre, Pebble Mill Road.

BLETCHLEY

8th. IEE — "Tomorrow's world and microwave communications" by P. J. Mountain at 19.30 at Post Office Training Centre, Horwood House.

BRIGHTON

13th. IEE — "Electro-acoustics" by Prof. E. Ash at 19.30 at the University of Sussex.

BRISTOL

5th. IEE — "Automobile Electronics" by C. S. Rayner at 18.00 at Mercury House, Bond Street.

8th. IEE — "Electronic calculators" by B. Clarke at 19.30 at Queens Building, Bristol University.

28th. IEE/IERE — "Marine electronics" by speaker from Marconi International Marine Ltd.

28th. IEETE — "Programmable logic controllers" by C. C. Cargill at 19.30 at Royal Hotel, College Green.

BURY ST EDMUNDS

7th. IEE — "Police Research" by B. J. Blain at the Angel Hotel.

DERBY

6th. IEE — "Automobile electronics" by D. B. Hodgson at 19.00 at the Lecture Theatre, College of Art and Technology, Kedleston Road.

DUBLIN

8th. IEE — "Electronic aids for medical studies" by Dr E. T. Powner and P. J. Best at 18.00 at Physics Laboratory, Trinity College.

DURHAM

5th. IEE — Exhibition and "Telecommunications; past, present and future" by W. J. Bray at Durham Castle.

EASTBOURNE

8th. IEETE — "Royal Greenwich Observatory" by G. H. Gill at 19.30 at The Drive Hotel, Victoria Drive.

EDINBURGH

8th. IEE — Symposium on "Further developments of applications of micro-computer systems" at 9.30 at Heriot Watt University, Grassmarket.

23rd. IEE — Faraday Lecture on "The entertaining electron" by F. H. Steele, afternoon and evening at The Usher Hall.

GLASGOW

21st. IEE — Faraday Lecture on "The entertaining electron" by F. H. Steele in the evening at The Kelvin Hall.

HATFIELD

6th. IEETE — EASCON 76 one-day conference "Links: education — employment" at Hatfield Polytechnic.

KINGSTON-UPON-THAMES

1st. IEETE — "The testing of electrical household appliances" by M. H. Hewett at 19.30 at Kingston Polytechnic, Penrhyn Road.

LIVERPOOL

5th. IEE — "Music hath charms . . ." at 18.30 at the Department of Electrical Engineering, Liverpool University.

LOUGHBOROUGH

27th. IEE — "Introduction of adaptive control techniques into areas of classical control" by J. R. Wolton at 19.30 at Lecture Theatre J002 Ed., Herbert Building, Loughborough University.

MANCHESTER

14th. IEE — "Microprocessors" by Prof. D. Aspinall at 18.15 at the University of Manchester.

MIDDLESBROUGH

7th. IEE — "Rapid fault finding techniques to minimise down time" by R. H. Baulk at 18.30 at Cleveland Scientific Institute, Corporation Road.

NEWCASTLE-UPON-TYNE

12th. IEE — "Colour TV — a popular approach" by G. D. Barnes at 18.30 at Room L101 Merz Court, University of Newcastle-upon-Tyne.

27th. IEE — Faraday Lecture on "The entertaining electron" by F. H. Steele, 19.15 at City Hall.

NOTTINGHAM

6th. IEETE — "Computerised control of Nottingham traffic" by M. B. Tate at 19.00 at New Mechanics Institute, St Trinity Square.

PORTSMOUTH

6th. IEETE — "Oracle — the teletext data broadcasting system" by G. A. McKenzie at 19.30 at Highbury Technical College, Cosham.

RUGBY

7th. IEE — "The future of the IEE" by R. J. Clayton at 18.30 at Lanchester Polytechnic, Rugby.

SHEFFIELD

20th. IEE — "Future role of the IEE by Dr E. Laverick at 19.30 at Sheffield University.

28th. IEE — "Electronic techniques in Archaeology" by Dr E. T. Hall at 18.30 at Sheffield Telephone House.

SWANSEA

8th. IEE — "Transducers for modern automobile systems" by J. Moore at 18.15 at University College.

SWINDON

6th. IEE — "Sonar and underwater acoustic communication" by V. G. Welsby at 18.15 at The College, Regent Circus.